Basic Four® Model 6400 Cartridge Tape Drive Service Manual

Basic Four Information Systems®

BFISD 8015B

Reprinted August, 1979
Revised June, 1980
Reprinted 1981

Printed in the United States of America

Basic Four Information Systems Division/Management Assistance Inc.
14101 Myford Road, Tustin, California 92680/(714) 731-5100

Basic Four® Model 6400 Cartridge Tape Drive Service Manual

BFISD 8015B

May 1983

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The Model 6400 Magnetic Tape Cartridge Drive (MTCD) records at 6400 bpi with a 9.2 megabyte tape cartridge. The recording format is four track serial, with a data transfer rate in both the read and write mode of 192,000 bits per second. An integral tape cleaner is provided. Track selection is performed by the Controller located in the CPU card cage. The MTCD provides backup data storage capability and an economical means of off-line storage of selected data (see Figure 1-1).

Figure 1-1. Magnetic Tape Cartridge Drive (MTCD)

1.2 PURPOSE

This Service Manual is the primary source of information for first level maintenance. It contains the necessary information to repair and maintain the MTCD. This manual contains both physical and functional descriptions, installation/operations, maintenance procedures, and equipment supplied.

This information shall enable a Service Engineer to identify, isolate, and repair the MTCD.

1.3 PHYSICAL DESCRIPTION

The MTCD is packaged as a single unit and is directly connected to the CPU main frame and placed on top of the cabinet. The MTCD is made up of a cabinet, power supply, tape drive, and a ANSI magnetic tape cartridge.

The Cabinet contains a standard ac to dc power supply (refer to Chapter 2, Preinstallation Checks, for 115 volts ac to 230 volts ac conversion). A transparent window is provided for visual inspection of the cartridge during normal operation. The opening for the tape cartridge is directly below the window.

1.3.1 TAPE DRIVE TRANSPORT

The Tape Drive Transport, hereafter referred to as Transport, will record and reproduce data onto and from Magnetic Tape Cartridges. The Transport consists of three subassemblies; Magnetic Head Assembly, Switch/Sensor Assembly, and Heat Sink Assembly. The Transport also contains a tape cleaner, capstan drive motor tachometer and houses the PCBs.

1.3.1.1 Magnetic Head Assembly

The Magnetic Head Assembly consists of a closed magnetic circuit. This circuit is built of laminated high permeability metal with wound coils for inducing and detecting flux reversals. It is constructed as a dual gap with erase head (read-while-write-while-erase). Control signals are received from the Controller located in the CPU card cage via an interface cable which enables it to write or erase as required.

1.3.1.2 Switch/Sensor Assembly

The Switch/Sensor Assembly contains circuitry to sense Beginning of Tape (BOT), End of Tape (EOT), Load Point (LP) and Early Warning (EW). This enables automatic tape positioning after cartridge insertion, power on, or a rewind operation. It further contains the File Protect and Cartridge-In-Place switches.

1.3.1.3 Heat Sink Assembly

The Heat Sink Assembly contains the drive motor/tachometer, power transistor circuits, and a two piece heat sink. It is designed as a plug-in-module and is center of gravity mounted.

CAUTION

The MTCD must be mounted in a horizontal position only. This prevents dust and residue from falling into the Transport which could result in lost data.

1.3.1.4 Tape Cleaner

The Tape Cleaner removes foreign material and loose oxide particles as the tape passes the Tape Cleaner.

1.3.2 MAGNETIC TAPE CARTRIDGE

The Magnetic Tape Cartridge Assembly is shown in Figure 1-5. Each Magnetic Tape Cartridge Assembly is a single assembly consisting of a supply reel (to left), take up reel (to right), a magnetic tape, file protect and belt guides.

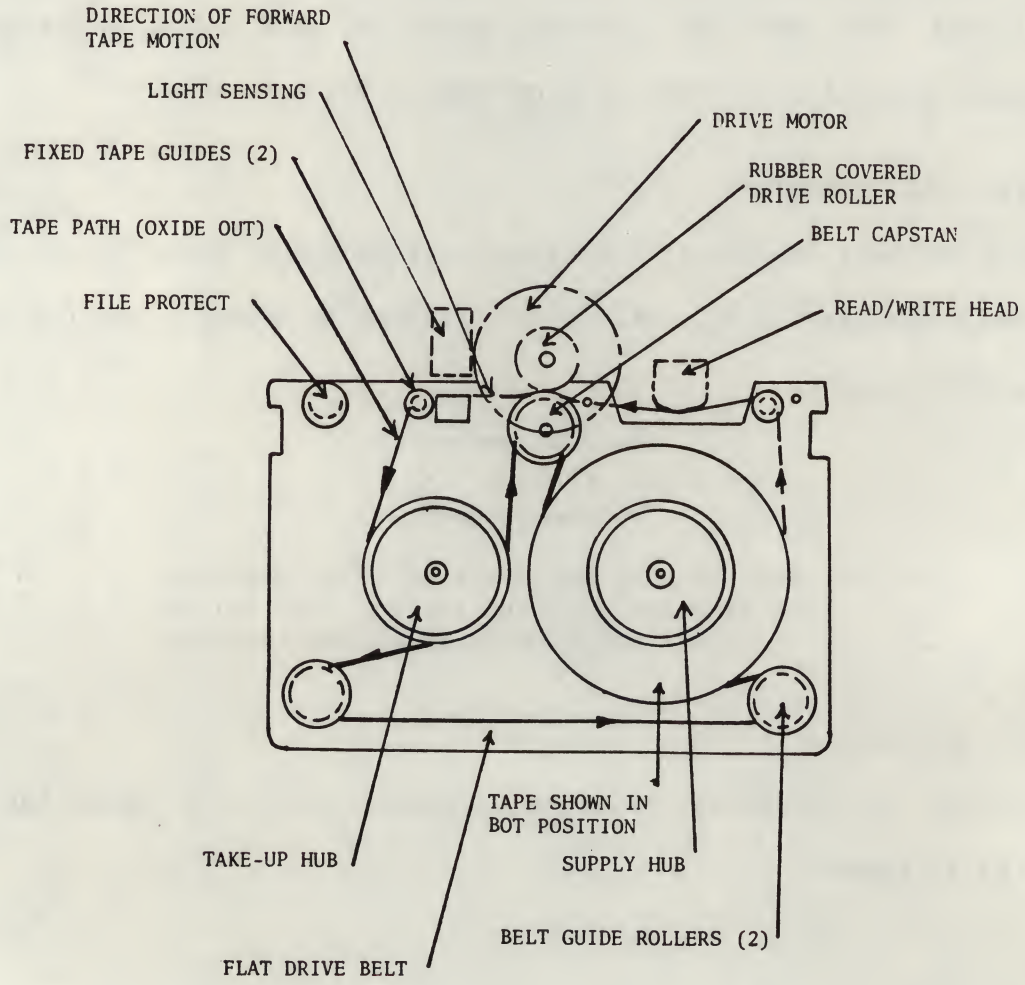


Figure 1-5. Cartridge Diagram

The Cartridge dimensions are shown in Figure 1-6.

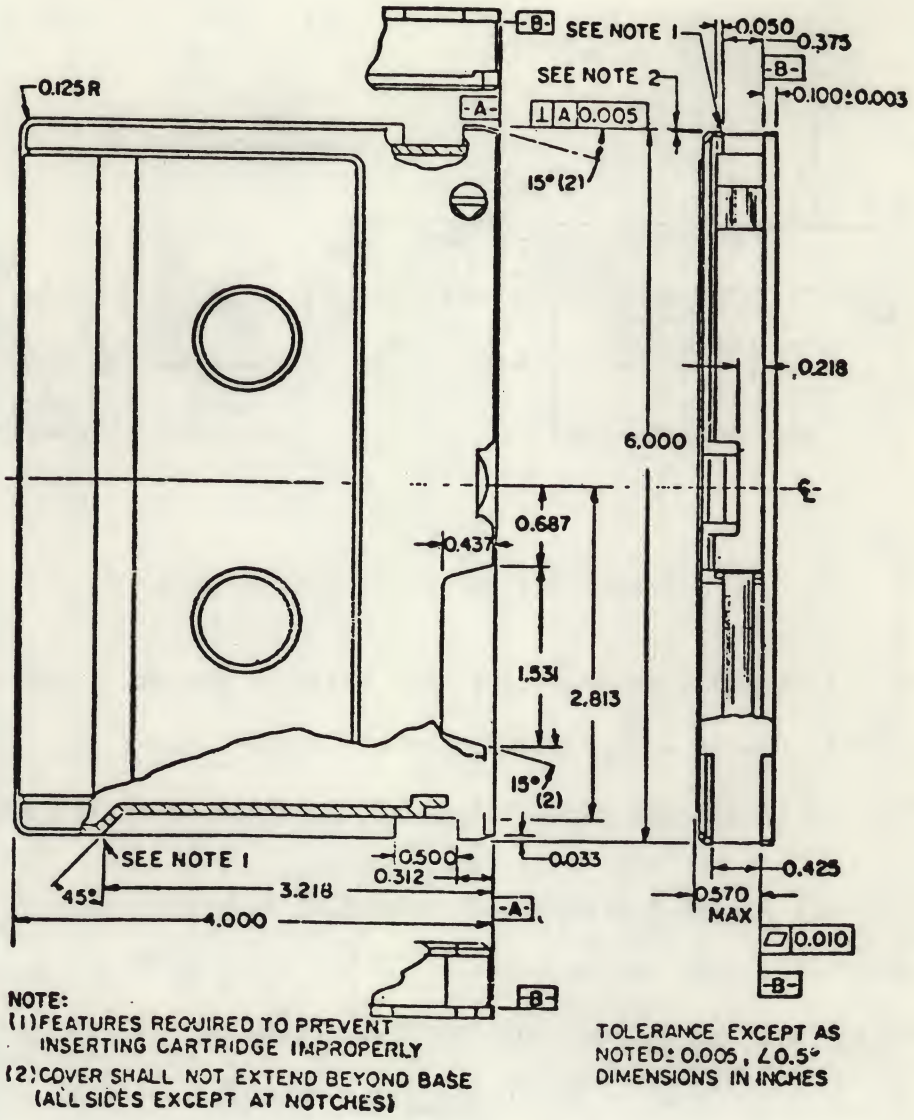


Figure 1-6. Cartridge Dimensions

The Cartridge is to be mounted in one position only and has asymmetrical features to prevent improper installation. The Cartridge contains optical elements to enable photo-electrical detection of tape position holes. The cartridge has a sensing area on the front surface which senses when the cartridge is in position to read or write (see Figure 1-7 for dimensions).

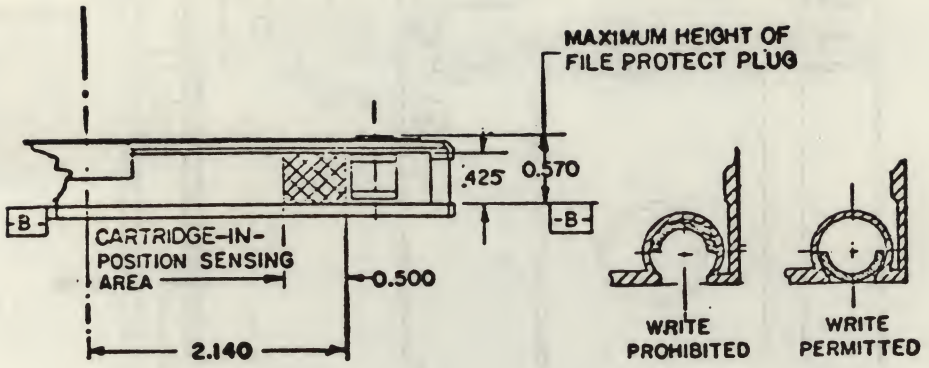


Figure 1-7. File Protect Switch

Tape guides are employed to guide the tape while in motion. The file protect cam of the cartridge is an operator rotatable switch (see Figure 1-5) which prevents writing or erasing when in the SAFE position (see Figure 1-7).

The magnetic tape length between Load Point (LP) and Early Warning (EW) shall be 300+10-0 feet. The tape position holes for Beginning of Tape (BOT), Load Point (LP), Early Warning (EW), and End of Tape (EOT) are shown in Figure 1-8.

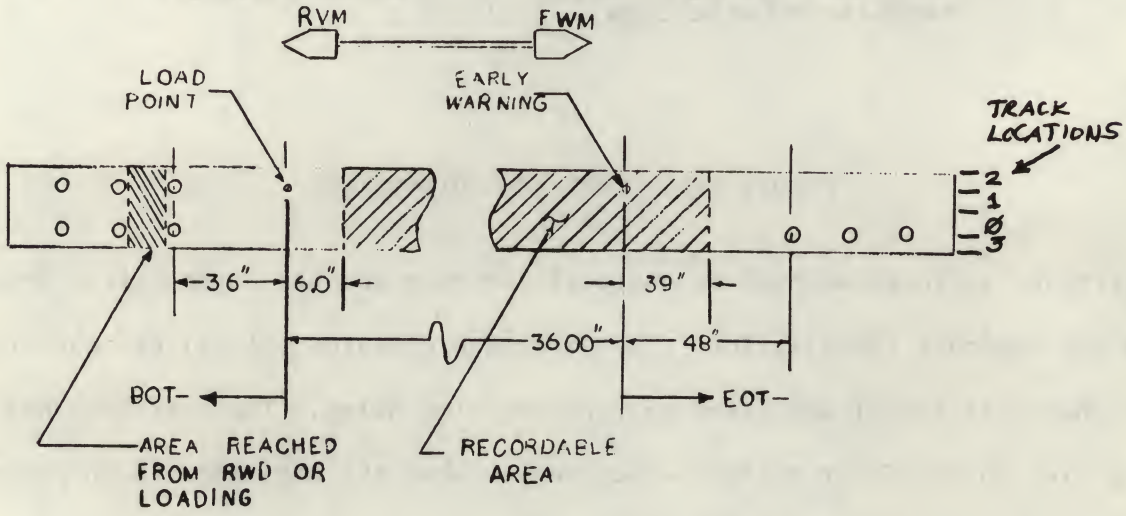


Figure 1-8. Tape Configuration

The presence of a spurious tape signal, after a tape has been erased, will not exceed 10 percent of the average base to peak read signal under test. The tape is wound on the reel with the magnetic coating out. During forward operation it will wind clockwise and unwind counterclockwise as viewed through the transparent door.

1.4 MTCD SPECIFICATIONS

Table 1-1 summarizes the general operation and performance of the MTCD. This table provides a reference source of general data for the Service Engineer.

TABLE 1-1. SPECIFICATIONS

Parameters	Characteristics
PHYSICAL	
Height	6.0 inches (15.2 cm)
Width	13.5 inches (34.3 cm)
Depth	12.0 inches (30.5 cm)
Weight	18.8 pounds (8.5 kg)
AC POWER REQUIREMENTS	
Voltage	115/230 VAC
Current	1.5/.75A
Power	172 VA
Frequency	60/50 Hz, 1 phase
Heat Output	586.5 Btu/hr
DC POWER REQUIREMENTS	
Voltage	+24 VDC ± 15% -24 VDC ± 15% +5 VDC + 5% - 3%
Current (Amperes)	+24 VDC: 1.8 typ; 3.4 max. -24 VDC: 1.9 typ; 3.5 max. +5 VDC: 1.4 typ; 2.6 max.
Drive Power Dissipation	18.5 Watts Typical Without Motion 57.4 Watts Typical With Motion 68.9 Watts With 10% Ramp Duty Cycle

TABLE 1-1. SPECIFICATIONS (continued)

Parameters	Characteristics
ENVIRONMENTAL REQUIREMENTS	
Temperature	65°F to 75°F (18°C to 25°C)
Humidity	40% to 60% RH non-condensing
Altitude	0 to 10,000 feet
MAGNETIC TAPE	
Read to Write Gap Spacing	.300 ± .005 inch
Write to Erase Gap Spacing	.300 ± .010 inch
Write Gap to EOT/BOT Optical C/L	2.50 ± .04 inch
Erase Track Width	.032 ± .005 inch
Write Track Width	.028 ± .002 inch
Read Track Width	.010 ± .002 inch
Tape Motion	Steady State
Bit Period Definitions	Speed Range: Low / High; Nominal Speed (ips): 30 / 90; Nominal Bit Period (microseconds): 5.208 / 1.74; Nominal Data Transfer Rate: 192,000 bps
ANSI Standard	ANSI Standard #X3B5/75-43
GENERAL	
Cartridge	ANSI x 3.55 - 1977 300' or 450' tape length
Recording Density	6400 bpi, MFM, or other high density codes
Recording Mode	4-Track Serial
Head Type	Dual Gap, Read-While-Write with Separate Erase
Tape Cleaner	Integral

TABLE 1-1. SPECIFICATIONS (continued)

Parameters	Characteristics
GENERAL	
Operating Speeds	30 ips Write, Bidirectional Read 90 ips Bidirectional Search and Rewind
Transfer Rate	192,000 Bits/Sec.
Start/Stop Time	At 30 ips: 0.30/0.41 inches At 90 ips: 2.97/3.42 inches
Instantaneous Speed Variation	±3% (Drive only, ±7% cartridge inclusive)
Long Term Speed Variation	±2% (Drive only, ±3% cartridge inclusive)
Data Reliability	Less than 1 Error in 10^8 Bits
Interface Signal Levels	Standard TTL Levels Logic 1 = 0.0 to +0.4 VDC Logic 0 = +2.4 to +5.0 VDC

CHAPTER 2

INSTALLATION AND OPERATION

INSTALLATION

2.1 UNPACKING/PACKING PROCEDURE

The MTCD is shipped as part of a system. Instructions for unpacking/packing as a part of a system are found in the system manual. This manual will cover procedures for the MTCD only.

2.1.1 TRANSPORT

The shipping container provides protection against moisture, dust, and contact damage. If the MTCD is not to be installed, but placed in storage, it should be opened and checked for damage, then repacked. Use the following procedure for unpacking/packing the MTCD.

1. Upon receipt of the shipping container, examine for damage, report any damage to the carrier before opening.
2. If no damage is noted, and the MTCD is not to be placed in storage, cut the packing tape on the top center of the container and open the outer container.

Use care when cutting the tapes to open the container. Too deep of a cut may damage cabinet or transparent door on the cabinet.

3. Cut packing tape on inner container, open container and lift out the MTCD or Transport.
4. Examine for damage, noting any dents, cracks, or missing parts per shipping list. If any are found, they should be reported to the Marketing Office or Dealer immediately.

CAUTION

Use care in removing the Transport. The Heat Sink and Pins are exposed. Mechanical damage can result if bent or broken.

5. All containers and packing material, especially preformed containers, must be saved. These are to be reused if the assembly is returned to the factory.

6. Packing is the reverse of the above procedure, using the saved container and packing material. Add packing tape to replace the cut tape in the unpacking procedure.

2.2 PREINSTALLATION CHECKS

The first part of this section will explain the procedure to install a Transport in the cabinet.

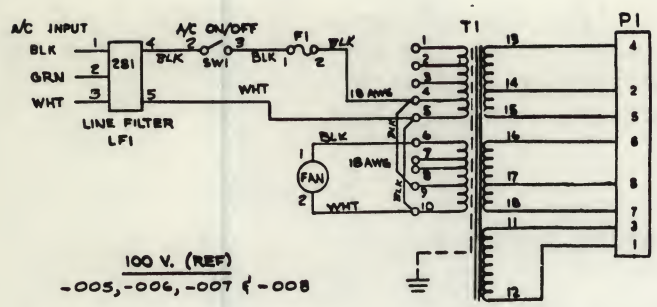
2.2.1 INSTALLING A TRANSPORT

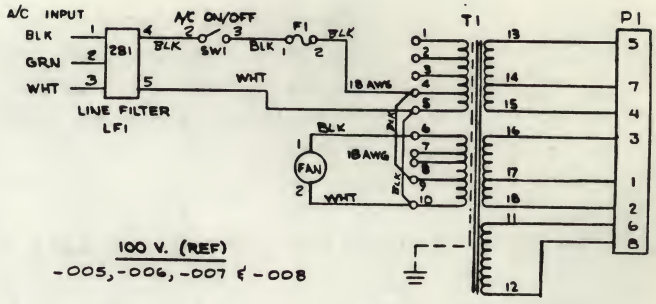
First, remove the top cover. In newer models, the top cover is held in place by stick-together clamps. Remove the transparent window, then lift up on the front of the top cover and it will snap loose. In older models, the cover is screwed down, remove the screws and then lift off the cover. This will expose the inner parts of the MTCD.

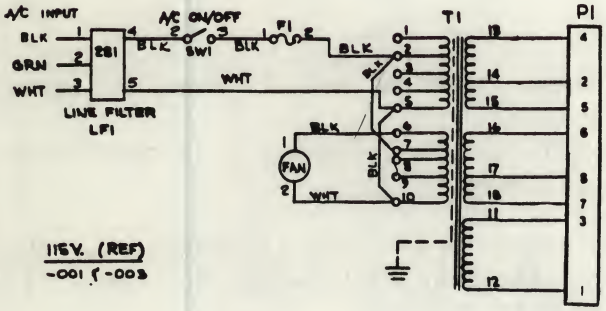
When installing the Transport, proceed as follows:

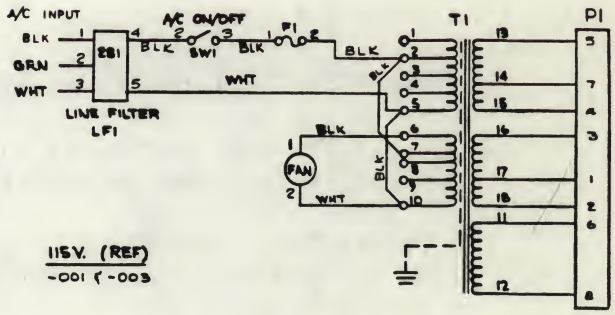
- If unit is still plugged in:
  1. Set ON/OFF switch on rear of lower cover to OFF.
  2. Remove ac power plug from ac outlet.
- Remove cables from PCB (Cartridge Tape Drive Power Supply) located at J1 and J3.
- Lift out the PCB (Cartridge Tape Drive Power Supply) and set aside.
- Place Transport in lower cover.

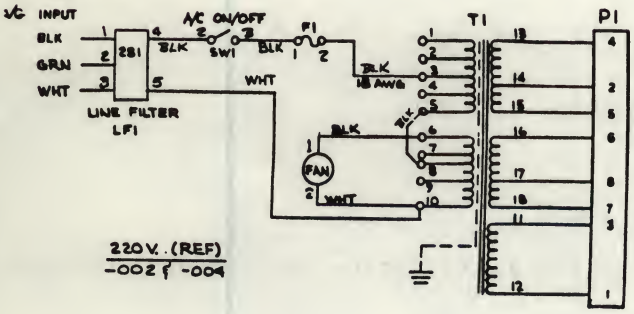
VENDOR VERSION











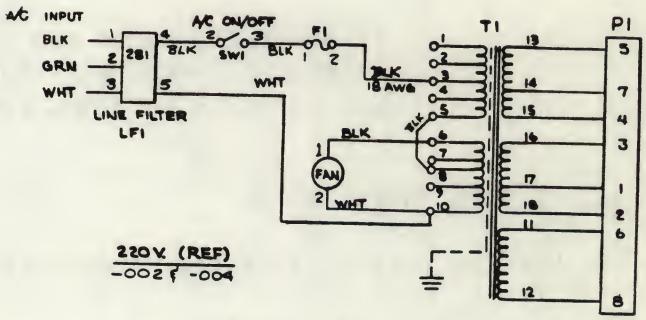


Figure 2-2. Converting From 100V to 220V

CAUTION

Clean heads carefully. Spray type head cleaners are not recommended as they may contaminate the drive motor lubricant. Cleaning the head with hard metal objects will result in permanent head damage.

The Tape Cleaner may be cleaned with a folded sheet of paper. Insert the folded paper into the open slit and move the paper up/down twice.

Install the transparent window, and insert a cartridge. Look through the transparent window and observe tape motion. Tape should move forward approximately one second and then reverse to BOT.

1. Grasp the tape cartridge firmly with one hand and pull it from the opening.
2. Place the tape cartridge in the opening and push forward till the stopping point is felt and an audible sound is heard.
3. Verify tape motion, if none; insure the ac power cord is connected, power is on, and the fuse is not blown. If the fuse is blown or the tape still does not move, refer to Chapter 4 of this manual.
4. If the tape is in motion and stops at BOT, the MTCD is ready for normal operation.

NOTE

If the tape was on the left reel (take-up), automatic rewind will take place till the tape has moved to the right reel (supply) and BOT.

2.3 SYSTEM INSTALLATION

The MTCD is part of a system, therefore the System Installation and Preinstallation Checks are one and the same.

2.4 SYSTEM INITIALIZATION PROCEDURES

2.4.1 BASS PROGRAM

1. Install a tape cartridge (scratch tape) in the Transport.
2. Perform an alternate load from disc (refer to Table 2-1).

TABLE 2-1 SENSE SWITCH SETTINGS (CPU)

Switches 1	2	3	4	Function
0	0	0	0	Fixed Media Load
0	0	1	0	Fixed Media Alternate Load
1*	1*	0	1	Tape Cartridge System Load**
1	1	1	1	Tape Cartridge Alternate Load
1	0	0	1	VDT Boot
0	1	0	1	Disc Load
0	1	1	1	Disc Alternate Load

*Test SW on front panel (CPU) may be used instead of SS3

**Not allowed in present operating system.

3. Press and release LOAD switch on processor front panel.
4. VDT displays the PROPRIETARY MESSAGE, then:

   MAKE ENTRY TO OVERRIDE DEFAULT

5. Within 10 seconds, press carriage return (CR)
6. VDT displays:

   ENTER PROGRAM NAME

7. Type BBIITC, then press carriage return (CR)
8. VDT displays:

   ENTER PROGRAM NAME (*MTC OR BASS)

9. Type BASS, then press carriage return (CR)

10. VDT displays:

```
BASIC FOUR ALL PURPOSE SERVICE SYSTEM

SYSTEM DATE IS:  XX/XX/XX
DO YOU WANT TO CHANGE IT?  (Y/N)
```

11. Type N, then press carriage return (CR)

12. VDT displays:

```
SYSTEM TIME IS:  XX:XX
DO YOU WANT TO CHANGE IT?  (Y/N)
```

13. Type N, then press carriage return (CR)

14. VDT displays:

```
1.  B/4 SERVICE SYSTEM
2.  INSPECTION CYCLE
3.  BURN-IN CYCLE
4.  DISPLAY/PRINT PREVIOUS TEST RESULTS

ENTER YOUR SELECTION (CR = END)
```

15. Type 1, then press carriage return (CR)

16. VDT displays:

```
WOULD YOU LIKE TO HAVE DESCRIPTIONS OF SELECTED
BASS PROGRAMS?  (Y/N):
```

17. Type N, then press carriage return (CR)

18. VDT displays a listing of all BASS tests followed by:

```
SELECT NUMBER(S):
```

19. Type 15 (write test) or 16 (read test), then press carriage return (CR)

20. VDT displays:

```
SELECTED ENTRIES:  15
ENTER ONE OF THE FOLLOWING:  (A = ADD, D = DELETE,
R = REVIEW, CR = EXECUTE):
```

21. Press carriage return (CR)

22. VDT displays:

```
DO YOU WANT TO LOG ERRORS TO THE ERROR FILE?  (Y/N)
```

23. Type Y, then press carriage return (CR)

24. VDT displays:

    DO YOU WISH TO RESET ERROR FILE? (Y/N):

25. Type Y, then press carriage return (CR)

26. VDT displays:

    %M11
    DESCRIPTION OF TEST
    ENTER TAPE CARTRIDGE UNIT TO TEST (CØ - C3):

27. Type CØ, then press carriage return (CR)

28. VDT displays:

    HOW MANY ERRORS TO BE DISPLAYED ON VDT?

29. Type 1Ø, then carriage return (CR)

30. At the completion of the test (approximately 10 minutes) the VDT shall display:

    DO YOU WANT TO TEST ANYMORE TAPE CARTRIDGE UNITS? (Y/N):

31. Type N, then press carriage return (CR)

CHAPTER 3

MAINTENANCE

3.1 CORRECTIVE MAINTENANCE

3.1.1 GENERAL PHILOSOPHY

This chapter contains information which will aid the Service Engineer in troubleshooting the MTCD.

3.2 TROUBLESHOOTING PROCEDURES

A typical sequence used to isolate the trouble to a replaceable module or PCB is as follows:

- Collect information about the malfunction.
- Examine the unit to see if power is applied.
- Examine for a blown ac line fuse.
- Decide if the malfunction is in the MTCD or the Controller.
- If the MTCD is bad, switch OFF power and open the cabinet.
- Examine for loose connectors or broken wires.
- Examine for broken or burned parts.
- If the malfunction is located, correct it.

3.3 FUNCTIONAL DESCRIPTION

The MTCD functions within a system as a backup read and write memory device. The record mode is four track serial. Data and control signals are received via an interface (I/O) cable connecting the MTCD to the CPU. The two major functional systems of the MTCD are the Power Supply and Transport. The Transport contains two sub-functions, they are; Tape Motion Control and Read/Write Operations.

3.3.1 POWER SUPPLY

The Power Supply is an open frame, multi-output power supply which supplies the Transport with its required dc voltages. Tap changes on the Transformer (T1) give the following ranges over a frequency range of 47 to 63 hertz (see Figure 2-2).

100 ± 10% VAC	200 ± 10% VAC
110 ± 10% VAC	220 ± 10% VAC
115 ± 10% VAC	230 ± 10% VAC
120 ± 10% VAC	240 ± 10% VAC

The Power Supply outputs the following voltages, including a regulated 5.0 volts dc ±0.1V. Measure voltage at TP4 on PCB. Adjust R5 for correct level.

±5V @ 2.6A
+24V @ 1.5A, with 3.5A surge up to 80 milliseconds
-24V @ 1.5A, with 3.5A surge up to 80 milliseconds

A crowbar overvoltage circuit is provided on the +5 volts output. The crowbar trips above 6.5 volts dc.

3.3.2 TRANSPORT

The Transport is made up of three assemblies and five PCBs dividing the Transport into two sub-functions. The two sub-functions are; Tape Motion Control and Read/Write Operations. The assemblies and PCBs are:

Assemblies	Printed Circuit Boards
Magnetic Head	Interconnect Board
Switch/Sensor	Data Circuit Board
Heat Sink	Interface Board
	Encoder/Decoder Board
	Servo Board

3.3.3 SUB-FUNCTIONS OF THE TRANSPORT

A functional description of the assemblies and PCBs that make up the Transport are best explained in the following sub-function descriptions.

3.3.3.1 Tape Motion Control

The Switch/Sensor Assembly, located on top of the drive, is used to determine the state of the tape cartridge and the position of the tape. The two microswitches in the Switch/Sensor Assembly are used to originate the Cartridge-In-Place (CIP) and File Protect (FIP) signals. CIP goes true whenever a cartridge is completely engaged. The FIP signal will be true only when the File Protect Indicator Arrow on the cartridge points toward the SAFE position. This will disable the write operation.

Upper Tape Hole (UTH) and Lower Tape Hole (LTH) signals are derived from two photo sensors. These signals go true whenever an upper or lower tape hole has passed the sensors.

These signals are sent directly to the Interface Board which utilizes the tape holes to control tape position. The tape cannot run forward beyond the second EOT hole or reverse past the second set of BOT holes.

3.3.3.2 Read/Write Operations

The Data Board contains a read envelope threshold detection comparator network to assure valid read data and to discriminate against non valid data. This network disables the Data Detected signal unless the read envelope exceeds a certain predetermined voltage. This voltage is 60 millivolts during normal read operations; 200 millivolts during a read after write operation (Write enable (WEN) true enables the 200 millivolts threshold); 500 millivolts during a high speed search (High Speed (HSP-) true enables the 500 millivolts threshold). The Read envelope threshold detector is used to produce the Data Detected (DAD) signal.

After the selected track on the read heads have been determined, the Read Data is input to a read amplifier, which amplifies the data to approximately 250 millivolts, and filtered by a low pass network. This MFM data, plus the Data Detected signal, is sent to the Encoder/Decoder Board via a line driver.

The Read Data decoding stages of the Encoder/Decoder Board include a desnake circuit (which eliminates data dropouts during periods of no transition), a phase lock servo, a timing pulse generator (consisting of four one-shots whose pulse widths are controlled by the servo output), and a data acquisition circuit (which strips the preamble and a Read Data Strobe generator .

The timing pulse generator (four one-shots) produce four sampling pulses of variable width. Each pulse is timed by the phase lock servo to equal one quarter of the bit cell. This division helps in the detection of the mid bit transition which is peculiar to "one" data bits of the MFM code. Depending on the data pattern, two of the sampling pulses (E0-A and E1-A) which represent 0 and 1 data bits are applied to the data acquisition network.

This network develops the NRZ data. The Read Data Strobe is developed by a flip-flop/nand gate combination that automatically eliminates the all-ones read preamble by disabling the Read Data Strobe during its occurrence.

3.4 ELECTRICAL ADJUSTMENTS (For information only. Not a field adjustment.)

3.4.1 GAIN ADJUSTMENT (DATA BOARD)

Adjust for a 1.9 volts dc positive and negative read envelope output on the lowest output signal track using the following procedure.

1. Using an external DEI 302030 Data Pattern Generator or its equivalent, write an "all ones" test pattern on all tracks in MFM format. (Data transfer rate is 192 kilohertz at 30 inches per second.) (Other data sources may be used and none is required in drives having Codec Boards.)

2. Read back each data track while alternately monitoring the positive or negative read envelopes on the Interconnect Board. Test points are J500-20 (positive envelope) and J500-3 (negative envelope) on the Interconnect Board. Determine track exhibiting lowest amplitude read envelopes.

3. Adjust pot R513 on the Data Board for 1.9 volts dc in the read reverse pass just after writing the track with the lowest amplitude.

4. Recheck all data tracks. Positive and negative read envelopes of each track should measure within ±0.05 volt dc of each other.

3.4.2 SERVO POWER ADJUSTMENT (SERVO BOARD)

Generally not required, unless a ±15 volts regulator has failed .

If failed, use the following procedure:

1. Connect VOM or DVM reference lead to diode VR700, cathode.

2. Attach VOM or DVM test lead to Pin 4 of operational amplifier U705. Record -15 volts dc voltage to three figure accuracy (XX.XXX).

3. Attach VOM or DVM test lead to Pin 7 of the operational amplifier U705.

4. Adjust R765 until +15 volts dc is within ±5 volts in positive direction of the reading obtained at Pin 4 of U705.

3.4.3 INTERFACE PCB ONE-SHOT PERIODS

LOCATION	PERIOD
U623 Pin 10	.9 ± .1 msec
U623 Pin 6	22 ± 5 usec
U617 Pin 6	650 ± 100 msec
U617 Pin 10	650 ± 100 msec
U614 Pin 3	30 ± 4 msec
U615 Pin 3	90 ± 15 msec

3.4.4 SERVO PCB POT SETUP

1. Adjust R761 for a voltage of 0.0 ± 0.1 volt at BALAS test point.
2. Set forward speed with R764. Set reverse speed with R763.
3. Adjust R762 for a ramp time of 23 ± 0.5 milliseconds.
4. Insure any loss of voltage that will result in loss of tape motion.

3.4.5 DATA ADJUSTMENT AND CHECK PROCEDURE

1. Write all "ones" pattern (192 kilohertz at 30 inches per second) on track 0. Unit select, track 0, forward, and write enable are required.

2. Attach scope probe to R535 on lead near R537 on board 301,061.

3. In the Read Only Mode, adjust R513, refer to 301,061 until the signal (approximately a sine wave in appearance) is 1.8 volts peak-to-peak.

4. Check inter-record gap voltage amplitudes after gain adjustment. Voltage shall not exceed 350 millivolts. All four tracks must be checked.

5. Check DAD signal to insure true level only during data.

   a. Attach scope trigger on forward command at P3, Pin 22 of PCBA 301,094. Observe DAD on U23, Pin 3 on PCBA 301,094. Place second (2nd) channel lead to R535 on LEAD NEAR R537 on PCBA 301,061 for data burst correlation.

   b. Operate drive in READ AFTER WRITE MODE and write at least 20 consecutive data blocks for check. All four tracks must be checked.

NOTE

First 100 microseconds after Forward Command may generate DAD spikes not of consequence.

3.5 PREVENTIVE MAINTENANCE

Preventive Maintenance which should be done by the Service Engineer is limited to cleaning as needed, and observing safety procedures while making repairs. Cleaning shall be done if the Transport is replaced.

3.5.1 MAGNETIC HEAD CLEANING

The Magnetic Head should be cleaned daily if the Transport is in regular use. Dirty heads may cause data dropouts during read and write operations. Use a non-residue, non-corrosive cleaning agent, such as DuPont Freon TF, and a lint free cloth to clean the head assembly. Be sure to wipe up any excess and allow the heads to dry prior to operating the Transport.

CAUTION

Spray type head cleaners are not recommended because overspray may contaminate the motor bearings. Also, never clean the head with hard metal objects. This will result in permanent head damage.

3.5.2 TAPE CLEANER CLEANING

The Tape Cleaner removes loose tape oxide and other foreign material from the tape before it contacts the head. This foreign material accumulates in and around the tape cleaner and must be removed to ensure that the Tape Cleaner will continue to work effectively. The Tape Cleaner should be cleaned on the same schedule as the head.

To clean, insert a folded sheet of paper in the bottom of the cleaning slot of the cleaner. Slide the paper up, lifting the foreign material from the cleaner. A soft brush may be used to remove the foreign material from the area around the tape cleaner and head assembly.

CAUTION

Do not use metal objects to clean the Tape Cleaner. If the Tape Cleaner should become scratched, it could scratch the tape surface, resulting in lost data.

3.5.3 MOTOR CAPSTAN CLEANING

The Capstan is composed of hard polyurethane and must be cleaned after foreign material has built up. Clean, using Freon and a lint free cloth. The cleaning schedule should be the same as for the head.

CAUTION

Be careful not to permit cleaning solvent to drip into the drive motor bearings as it will result in a failed component.

CHAPTER 4

REMOVAL/REPLACEMENT PROCEDURE

4.1 SPARE PARTS LIST

TABLE 4-1. SPARE PARTS

BFC MM	Vendor	Description	Quantity
160189	MDX-04.000	FUSE, 4A-MDX SB	5
160190	MDA-12.000	FUSE, 12A MDA	5
610010	B903030	PCB, CART TAPE CONTROLLER	1
610020	NB903040	PCB, CART TAPE POWER SUPPLY	1
610710	900960-002	CABLE, CARTRIDGE TAPE	1
611000	902761-001	TAPE DRIVE TRANSPORT	1
617010	345002	FAN, COOLING	1
617020	100321	SWITCH, TOGGLE	1
617030	180007-001	TRANSFORMER	Ø
737020	181003	RFI, FILTER	1

4.2 REMOVAL/REPLACEMENT PROCEDURE

This section explains the procedure to remove the major (spared) assemblies and install their replacements. Before removing any assembly, the following steps shall be followed:

- Remove Magnetic Cartridge
- Set power switch to OFF position
- Unplug the ac power cord from its source

4.2.1 PCB CARTRIDGE TRANSPORT POWER SUPPLY

This PCB is removed in the following manner:

- Complete steps in Section 4.2.
- Lift off the top cover of the MTCD (older models have screws holding them in place of the (3M) stick-tight connections). These screws must be removed to remove the top cover.
- Locate the PCB.
- Disconnect the cable at J1.
- Lift up on the PCB till the connectors J2 and J3 can be seen.
- Disconnect the cables at J2 and J3.
- Remove the PCB.
- To install a new PCB, repeat the above in reverse order.
- Verify the regulated +5 volts is within tolerance (refer to Section 3.3.1).

4.2.2 TRANSPORT

To remove the Transport, first complete the steps in Section 4.2, then do the following procedure.

- Remove the screws located on the bottom of the MTCD.
- Lift off the top cover.
- Disconnect the PCB Cartridge Tape Drive power supply and remove per Section 4.2.1.
- Lift the Transport up and to your left, placing on right side of MTCD.
- Disconnect cable at P702 of Servo PCB.
- Disconnect the I/O cable at P3 of Encoder/Decoder PCB.
- Lift the Transport up and set to one side.
- To install the Transport repeat the above in reverse order, connecting cables as required. Place top cover in place and tighten all screws loosened or removed.

CHAPTER 5

REFERENCE DATA

5.1 PURPOSE

This section contains Logic Diagrams, Schematics, and drawings used in the MTCD and is intended to be used ONLY by Service Engineers as a troubleshooting aid.

Tape Motion

Signal	Name	Description
FWD-	Forward	When true, causes the tape to move in a forward direction.
REV-	Reverse	When true, causes the tape to move in a reverse direction.
HSP-	High Speed	When true, causes the tape to move at high speed in the direction selected by either FWD- or REV- Tape motion will proceed until the command signals go false or: a. In forward where an EOT hole is encounted whereupon motion will stop. b. In reverse where a set of BOT holes is encountered whereupon motion will stop. c. Both directions are commanded simultaneously whereupon the tape will stop. d. Rewind command is received which will overrule other motion commands. e. Internal Ready signal is not true whereupon motion will stop. f. In High Speed, motion will drop to low speed when the upper "load point" hole is sensed in reverse or the upper "early warning" hole is sensed in forward.
RWD-	Rewind	When true, causes the tape to be positioned to beginning of tape at high speed. The Tape Drive must be selected to start a Rewind sequence, but may be unselected after the sequence is started. Beginning of tape is defined as between the two innermost (toward the middle of the tape) set of upper and lower holes located at the "head end" of the tape. This location is recommended for unloading the cartridge as the data recording area is completely protected. Rewind will "overrule" all other motion signals. Successive Rewind commands will not cause the tape to be "run off". Rewind will stop if the internal Ready signal is false. An automatic Rewind sequence is executed when a cartridge is installed in the Tape Drive or when power is applied when a cartridge is installed.

Input Data

Signal	Name	Description
WEN-	Write Enable	When true, enables the writing and erasing functions for the selected track. The writing and erasing processes occur only if the cartridge is in the unprotected state (not safe). This signal is internally latched and will remain set unless reset by: -Reverse or High Speed commands -Internal Ready signal, not true.
WDA-/ WDA+	Write Data	Will modulate the write head to produce a recorded waveform on tape when WEN- is true and the cartridge is in the unprotected state (not safe). In WDA+ (unactuated) state, the tape will be erased in the ANSI fashion. The WDA- state will cause the opposite polarity to be recorded. Therefore, if no erase head is used, erasing can be done by using the write head. The minimum clock period for data input should not allow the resultant number of flux reversal from exceeding 3200 per inch (1260 flux reversal/cm) and the rise and fall times should not be greater than 0.5 microseconds.

Output Status Signals

Signal	Name	Description
SLD-	Drive Selected	Will be true when the Tape Drive has received its proper unit address.
RDY-	Drive Ready	Will be true when a cartridge is installed, the sensor lamp is drawing current, and the +5 VDC is applied to the Tape Drive.
BSY-	Drive Busy	Will be true when the Tape Drive is in an automatic rewind sequence (i.e. when a cartridge is first installed in the Tape Drive), or when the Tape Drive is executing a rewind, forward, or reverse command. This signal will go true when the command is received and will remain true until the motion has stopped (i.e. 30 milliseconds after low speed motion has been commanded to stop and 80 milliseconds after 90 ips operation has been commanded to stop). In the case of receipt of a non-executed or illegal command, (FWD at EOT or REV at BOT), this signal will not be true, indicating the command is rejected.
FLG-	Flag	Will be set and latched when an automatic sequence to position the cartridge to BOT has been executed, or a rewind has been completed. This signal is reset by subsequent receipt of a FWD command.
WND-	Write Enabled	Will be true when a write enable condition is latched within the Tape Drive.
FUP-	File Unprotected	Will be true when a cartridge is installed and it is in the unprotected state (i.e. can be written on).
LPS-	Load Point Sensed	Will be set and latched when the upper load point hole (the warning of beginning of tape) is passed in the reverse direction. This signal will be internally reset when the load point hole is subsequently passed in the forward direction. When this signal is true, high speed will be disabled. Reverse tape motion is allowed to proceed until the BOT holes are encountered where the Tape Drive will stop and accept only forward commands.
EWS-	Early Warning Sensed	Will be set and latched when the upper early warning hole (the warning at end of tape) is passed in the forward direction. This signal will be internally reset when the early warning holes is subsequently passed in the reverse direction. When this signal is true, high speed is disabled. Forward tape motion is allowed to proceed until the EOT hole is encountered where the Tape Drive will stop and accept only reverse commands.

Output Data .

Signal	Name	Description
RDA	Read Data	This signal is a replica of the WDA data written onto the tape. The RDA line is latched and its initial state is not preset, thus, initially the RDA line may be high or low. Conditions can occur wherein single transitions can occur during erased portions of the tape. These can set the RDA line in the opposite state. The read signal is always available in dual gap drives, and is always available when WEN has been set for single gap drives. The threshold levels are internally set as a function of the mode of operation.

NOTE

Tape Drives with Encoder/Decoder circuit board assemblies have interface signals the same as serial Tape Drives equipped with interface circuit board assemblies, except the WDA and RDA signals

Input Data For Drives With an Encoder/Decoder Circuit Board Assembly

Signal	Name	Description
WDE-	Write Data Enable	A control line to the Tape Drive which separately allows enabling of the write function (the sending of write data strobes and the writing of data on tape). The WEN function is still required and will enable both writing and erasing. WEN causes the write circuits to become active and tape to be erased, after the tape is up to speed and other conditions met, the WDE will cause the Tape Drive to send the first data strobe and shall commence to record flux transitions on the tape. All data which is to be written on the tape must be sent to the Tape Drive (all preambles, postambles, and check characters) and that data is recorded in Manchester form, phase encoded.
WNZ-	Write Non-Return Zero Data	During the write data strobe period the state of the input write data line is sensed as follows: WNZ = Low = 1, and WNZ = High = 0 The state of WNZ is only examined during the write data strobe period. The WNZ signal must be steady 0.5 μsec prior to the the Write data strobe true period (WDS = Low).

Table 3-10. Ouput Data For Drives With an Encoder/Decoder Circuit Board Assembly

Signal	Name	Description
DAD-	Data Detected	Will be false except when data has been detected. Data detected requires the receipt of at least 12 zeros and a one following without a period of 2.5 bit times without data being received. Data detected can be used to sense the presence of the block of data. This signal will strip the preamble from the read data signal and is used to enable the other data output signals.
RNZ-	Read Non-Return to Zero Data	During read data strobe period if RNZ is low (true) then the data is a one, if high then the data is zero.
RDS-	Read Data Strobe	Will be low for 0.3 ±50% μsec indicating that RNZ can be sampled during this period. Read data in the forward direction will have preamble removed and will stay true for all of the postamble and for approximately 2.5 bit times after postamble has passed. (Therefore, CRCC and postamble must be stripped in forward direction and the CRCC and preamble must be removed in the reverse direction.) To first set read data, 12 zeros must be sensed. A drop-out will shut off circuit if it exists for >2.5 bit times (50 μsec) and circuit will stay off for 13 bit times (≈290 μsec). The read data threshold levels are internally set to three different levels depending on the write and motion commands. Read only threshold occurs when running at low speed without writing. Write threshold occurs when writing. Search threshold occurs when running at high speed.
WDS-	Write Data Strobe	The write data strobe is generated within the encoder/decoder module and is sent out to indicate when the Tape Drive is taking data. The low or true strobe period is 5.2 ±5% μsec.

APPENDIX A

MAGNETIC TAPE CARTRIDGE CONTROLLER

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1

INTRODUCTION

A1.1 GENERAL DESCRIPTION

The Magnetic Tape Cartridge Controller is a standard size Basic Four printed circuit board (PCB). This PCB is located in the card cage (CPU Backplane) of the CPU. For a typical system interconnection diagram, see Figure A1-1.

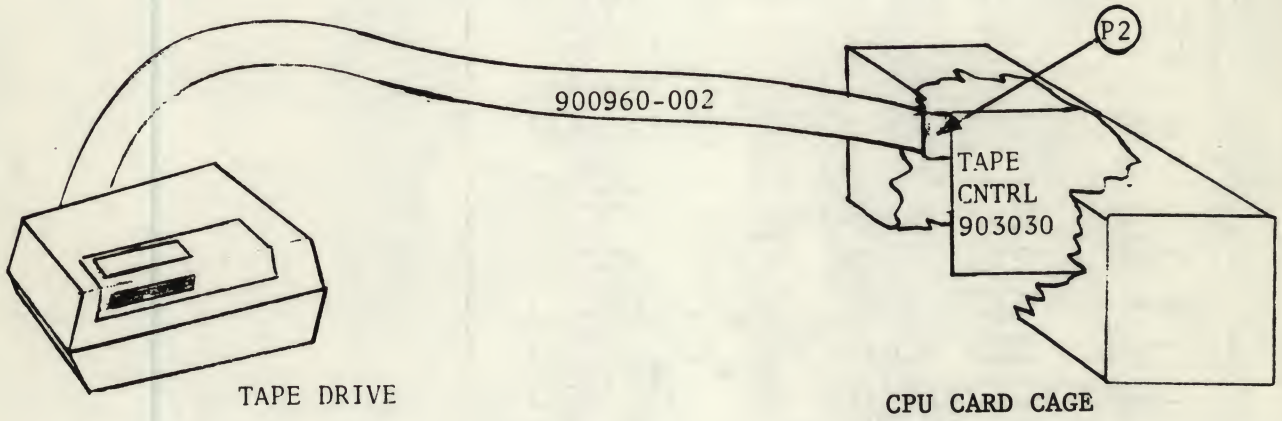


Figure A1-1. Magnetic Tape Cartridge/Controller Interface Cabling

A1.2 PHYSICAL DESCRIPTION

The Magnetic Tape Cartridge Controller, hereafter referred to as the Controller, is a single PCB plugged directly into the card cage of a processor system. A single interface cable (part number 900960-002) connects the Tape Drive and CPU Backplane. For drawing of the Controller PCB, see Figure A1-2.

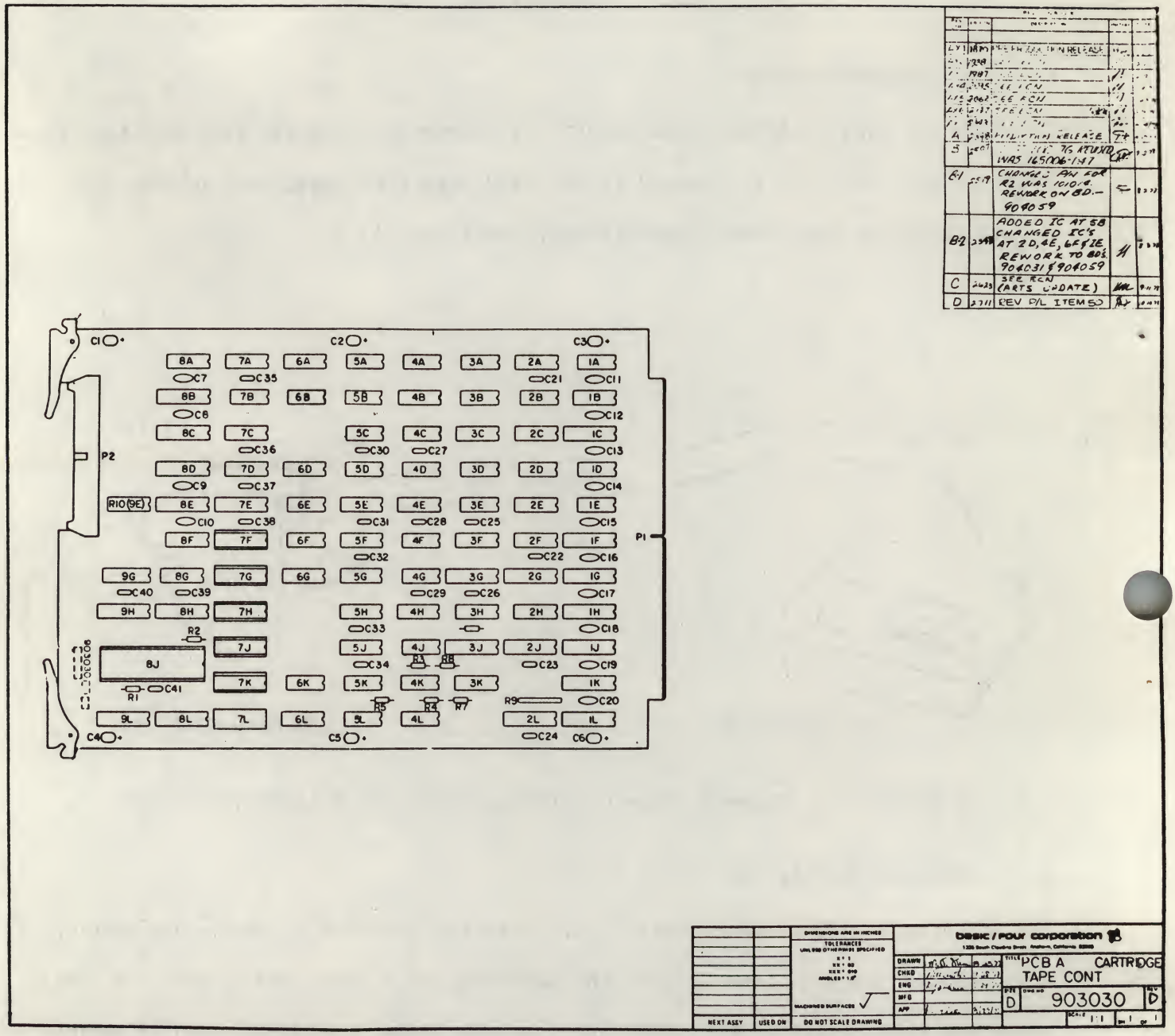


Figure A1-2. Controller PCB

The Tape Unit Interface Signal List is contained in Table A1-1.

TABLE A1-1. TAPE UNIT INTERFACE SIGNAL LIST

Pin	Signal	From	Comments
22	SLD-	Drive	Selected
4	RDY-	Drive	Ready
6	WND-	Drive	Write Enabled
8	FLG-	Drive	Flag
10	LPS-	Drive	Load Point Sensed
12	FUP-	Drive	File Unprotected
14	BSY-	Drive	Busy
16	EWS-	Drive	Early Warning Sensed
18	RWD-	Controller	Rewind
20	REV-	Controller	Reverse
22	FWD-	Controller	Forward
24	HSP-	Controller	High Speed
26	WEN-	Controller	Write Enable
28	SL1-	Controller	Unit Select 2^0
30	SL2-	Controller	Unit Select 2^1
32	SL4-	Controller	Unit Select 2^2
34	SLG-	Controller	Select Gate
36	RNZ-	Drive	Read NRZ Data
38	RDS-	Drive	Read Data Strobe
40	DAD-	Drive	Data Selected
42	WDE-	Controller	Write Data Enabled
44	WNZ-	Controller	Write NRZ Data
46	TR2-	Controller	Track Select 2^1
48	WDS-	Drive	Write Data Strobe
50	TR1-	Controller	Track Select 2^0

The MTCD pin-to-pin listing of the interface cable is shown in Figure 2-4.

The Computer Interface Signal List is contained in Table A1-2.

TABLE A1-2. COMPUTER INTERFACE SIGNAL LIST

Signal Name	Type	A Pin	B Pin
Master Reset	TTL Input	A-6	B-44
Clock Phase 1	TTL Input	A-6	
Clock Phase 2	TTL Input		B-22
I/O Control Reg 1	TTL Input		B-31
I/O Control Reg 2	TTL Input	A-31	
I/O Control Reg 3	TTL Input		B-61
Output Data Bit 0	TTL Output Bus		B-39
Output Data Bit 1	TTL Output Bus		B-10
Output Data Bit 2	TTL Output Bus	A-26	
Output Data Bit 3	TTL Output Bus		B-58
Output Data Bit 4	TTL Output Bus		B-37
Output Data Bit 5	TTL Output Bus	A-10	
Output Data Bit 6	TTL Output Bus		B-26
Output Data Bit 7	TTL Output Bus	A-58	
Input Data Bit 0	TTL Input Bus		B-32
Input Data Bit 1	TTL Input Bus	A-60	
Input Data Bit 2	TTL Input Bus		B-62
Input Data Bit 3	TTL Input Bus	A-62	
Input Data Bit 4	TTL Input Bus	A-32	
Input Data Bit, 5	TTL Input Bus		B-59
Input Data Bit 6	TTL Input Bus	A-61	
Input Data Bit 7	TTL Input Bus		B-60
Priority In	TTL Input		B-54
Priority Out	TTL Output	A-55	

TABLE A1-2. COMPUTER INTERFACE SIGNAL LIST (continued)

Signal Name	Type	A Pin	B Pin
Select In	TTL Input		B-52
Select Out	TTL Output	A-52	
External Interrupt Request	TTL Output	A-38	
+5 Volts DC	Power		B-1
			B-2
			B-64
			B-65
Ground	Return	A-1	B-19
		A-2	B-35
		A-13	B-36
		A-14	B-56
		A-18	
		A-33	
		A-34	
		A-56	
		A-64	
		A-65	
Memory Address Bit 0	TTL Output Bus		B-51
Memory Address Bit 1	TTL Output Bus		B-53
Memory Address Bit 2	TTL Output Bus		B-55
Memory Address Bit 3	TTL Output Bus	A-50	
Memory Address Bit 4	TTL Output Bus	A-53	
Memory Address Bit 5	TTL Output Bus	A-54	
Memory Address Bit 6	TTL Output Bus	A-15	
Memory Address Bit 7	TTL Output Bus	A-9	

TABLE A1-2. COMPUTER INTERFACE SIGNAL LIST (continued)

Signal Name	Type	A Pin	B Pin
Memory Address Bit 8	TTL Output Bus		B-14
Memory Address Bit 9	TTL Output Bus	A-11	
Memory Address Bit 10	TTL Output Bus	A-12	
Memory Address Bit 11	TTL Output Bus		B-13
Memory Address Bit 12	TTL Output Bus		B-7
Memory Address Bit 13	TTL Output Bus		B-18
Memory Address Bit 14	TTL Output Bus		B-9
Memory Address Bit 15	TTL Output Bus		B-47
Memory Address Bit 16	TTL Output Bus		B-33
Memory Address Bit 17	TTL Output Bus		B-41
Memory Data Bit 0	TTL I/O Bus		B-34
Memory Data Bit 1	TTL I/O Bus	A-35	
Memory Data Bit 2	TTL I/O Bus		B-43
Memory Data Bit 3	TTL I/O Bus		B-28
Memory Data Bit 4	TTL I/O Bus	A-36	
Memory Data Bit 5	TTL I/O Bus		B-30
Memory Data Bit 6	TTL I/O Bus		B-40
Memory Data Bit 7	TTL I/O Bus		B-27
DMA Acknowledge	TTL Input	A-57	
DMA Request	TTL Output	A-44	
DMA Memory Address Bit 15	TTL Output Bus		B-57
Read Enable	TTL Output Bus		B-23
RTXX-	TTL Input		B-20
Transmitted DMA Acknowledge	TTL Output		B-48
High Speed DMA	TTL Output Bus	A-24	

A1.2.1 FIRMWARE DESCRIPTION

The firmware is divided into two portions:

1. The Control Structure - includes power-on-sequencing, initialization, "Executive" idle loop and all paths in and out of the "Executive".

2. Command Sequencing - routine which realizes the Controller commands.

A1.2.1.1 Control Structure

- INIT - this routine begins at address 000_{16}. A Controller Reset (caused by I/O bus signal RESET - being asserted or by software issuing a Reset Control operation) forces firmware to begin executing at INIT as soon as the reset condition is removed. INIT performs the Controller Initialization.

  First, Controller status is set to FF, then all used ROM locations are added together (Modulo 256) and compared with an expected sum stored in ROM location KSUM. If the two sums are the same, then the Read/Write memory is tested. Each memory location is tested to verify that the following patterns can be written and read from it: 00, FF, AA, 55, and XY (XY is the 8 LSB of the memory location's address). If these tests also succeed, the firmware sets the Controller status to 00 and proceeds to START.

- START - various Read/Write Memory locations are set to 0. The Z80 interrupt mode is set to 1. The Z80 stack pointer is set to CFF_{16} (the top of Read/Write Memory). The Z80 H1 register pair is cleared and the "Executive" idle loop, EXEC, is entered.

- EXEC - this routine provides the main control structure of the operational firmware. When entered via "START", EXEC has nothing to do, so it loops (testing several internal and external flags) looking for things to do. One flag may be set by the Controller's I/O bus hardware, Command Received. (This flag is included as bits 5 of Input Port 27_{16}.) Two internally-created situations, caused by previously issued commands, are also tested as follows:

  1. When processing a Rewind command, the firmware merely initiates the Rewind, sets an internal flag to indicate the unit is rewinding and returns to EXEC (up to four units may be rewinding simultaneously). EXEC, then, will test the status of a rewinding unit until it reaches Beginning of Tape (BOT), at which point an interrupt will be initiated for that unit.

  2. Most Controller interrupts are processed through subroutine "SUINT". As described in the discussion of that routine, interrupts may be disabled by the executing software. If so, the Controller firmware will set a flag indicating an interrupt is "queued" and will return to EXEC. EXEC will monitor the two interrupt enable flags (Attention and Command Complete, bits 6 and 7 of Input Port 27_{16}). When an interrupt is re-enabled and a corresponding interrupt is queued, EXEC "unqueues" the interrupt and branches to "SEXIN" which performs the interrupt of the CPU.

- ECMDD - when a command is received, EXEC branches to this routine. This routine first sets the Controller's main status to "Busy" (by writing an 80_{16} to Output Port 20_{16}), then reads the command byte from Input Port 20_{16}. The four most significant bits (comprising the CMD field) are then used to branch, thru a table, to the routine which is coded to perform that command.

- SQINT - this subroutine is called by most routines at the completion of their normal operation or to abnormally abort a command. Two types of interrupts are defined in the product specification, Attention and Command Complete (which are essentially non-data-transfer and data-transfer-interrupts). Each may be selectively enabled or disabled by software. For each interrupt request, SQINT tests the associated enable/disable bit in Input Port 27_{16} (bit 6 for Attention, bit 7 for Command Complete). If enable, control is passed to "SEXIN". If disabled, an interrupt of the appropriate type is queued and control is returned to the calling routing.

- SEXIN - this subroutine, updates the Main and Auxiliary status bytes (and makes the Controller "Not Busy"). The interrupt requests flip-flop input to the CPU, it is then set by simply writing to Output Port 25_{16}, and is reset by the CPU acknowledging the interrupt. Control is then returned to the calling routine.

- EIPL, EIPLI - these routines initiate and control the firmware sequencing through the IPL sequence.

A1.2.1.2 Command Sequencing

Non-Data-Transfer Commands

The following routines are used to perform the set of non-data-transfer commands defined for the Controller.

They include certain subroutines which deal with the tape unit control and status lines. These routines are used by most of the major command-performing firmware routines.

- EILL - an illegal command status is posted, then control is passed to SQINT.

- ECLRI - any queued interrupts are removed from the queues. The status of the tape unit whose number is coded in the command is placed into the main and auxiliary status bytes. The Controller is made "Not Busy", and control is passed to EXEC.

- EREW - (Rewind). The last used track for the desired track is selected, then the unit's status is tested. If the unit is not ready, an abnormal termination exit is taken. Otherwise, the Rewind line to the unit is pulsed and control is returned to EXEC.

- EUNLD - (Unload). Similar to Rewind, except that the tape unit "Unload" control line is raised until the unit reaches End of Tape (EOT) (which is signified by the unit becoming "Not Busy"). Control is then passed to SQINT.

- ESP - all space commands cause control to be passed to this routine (Space File and Record, Forward and Reverse). Subroutines SELU and SREADY are called to select the unit and verify it is selected and ready. SBOT is called to check for reverse motion requested with tape positioned at BOT. Then routine SMOT is called to initiate tape motion. When tape is up to speed, subroutine SDAD is called to wait until data from tape is detected (i.e., the start of a record). Then, depending on forward or reverse motion, ESPFWD or ESPREV is entered. These routines read the first data bytes from tape and test for a value of 0. If 0, the record is a "File Mark". Control is passed to EFM where tape motion is stopped, a File Mark status is posted, and control is passed to SQINT.

  If not a File Mark, control is passed to ESPI to wait for the record to pass. If the command is a Forward File or Reverse File command, then the firmware loops to space over the next record until a File Mark is reached.

  If a Forward Record or Reverse Record command, tape motion is stopped, normal status is posted, and control is passed to SQINT.

Data Transfer Commands

The following routines perform the read, write, and data test command set of the Controller.

- EWRT - (Write, Write Gap, Write File Mark). All write-oriented commands enter this routine. Write Gap and Write File Mark proceed similarly to the space commands (see ESP above), except that: (1) the Tape Unit's Write Enable line is activated prior to initiating tape motion, (2) the INIT flip-flop is toggled to reset the write bit counter and various control terms in the tape unit interface logic and, (3) the last flip-flop is set in preparation for initializing the write CRC generation chip. Then, based on the command code, either EWG or EWRT2 is entered.

  EWG (Write Gap) - this routine simply delays enough time for about 4 inches of tape to be erased. Tape is stopped, their SQINT is called.

  EWRT2 (Write File Mark) - see the discussion of this routine below for the Write command.

  For Write Data, start up is different. The firmware must fetch the control block from main-frame memory (using subroutine "SGETCB") to establish the number of bytes to write and where the data buffer is in memory. Tape motion is then initiated ("SMOT") and control is passed to "EWRT2".

- EWRT2 (Write) - the write function can be broken down into three main portions: (1) front of record, (2) body of record, and (3) end of record. Front - this portion of firmware must write the preamble, initialize the CRC generator, and write the Leader on tape.

- ERSS, ETST, ERD - after write, these are anticlimactic.

Subroutines

These routines are used by many of the above described routines.

- SELU, SELUA - sets the track and unit numbers on the tape unit interfaces, then asserts the select line, thereby "selecting" the desired unit.
- SELUA - selects the track last used on the unit.
- SELU - selects the track specified in the command.
- SREADY - tests that the selected unit is selected, "Ready", and not Rewinding. If not, a not ready exit is taken, posting an abnormal condition status and calling SQINT.
- SGETCB - fetches the 7 byte control block (CB) from main memory by reading addresses 70_{16} - 76_{16}. It then places the address portions of the CB in the DMA Address Register and returns with the byte count in the DE register pair, the 16 address LSBs in the HL pair and the Index bytes in Read/Write Memory.
- SMOT - starts tape motion, providing appropriate delays to ensure proper gap size and proper head positioning before tape is written or read. SMOT tests for forward or reverse tape motion, setting the appropriate control signal to the selected tape unit. After SMOT commands the units to Move, it samples the units BSY (busy) status to insure it goes busy - if not, tape is either at physical EOT (forward motion) or BOT (reverse motion). If this occurs, control is not returned to the calling routine, instead the status is updated to reflect an "error" exit to "IERR3A".
- SDAD - this routine simply tests the tape units Data Detected (DAD) which is connected as bit 1.
- SBOT - test for BOT. This routine aborts reverse motion commands issued to a unit positioned at BOT and insures that the Load Point area of the Tape is not used by any of the forward commands.

A1.3 PHYSICAL REQUIREMENTS

The Controller will be installed in the card cage of a standard Basic Four data processing system. All clearance and airflow provisions normal to the Basic Four system will be observed.

A1.3.1 GENERAL SPECIFICATIONS

The general specifications including Electrical, Interface, and Environmental are listed in Table A1-3.

TABLE A1-3. GENERAL SPECIFICATIONS

Parameters	Characteristics
ELECTRICAL REQUIREMENTS	
DC Voltage	+5 V ± .25 V
DC Current	3.8A
INTERFACE REQUIREMENTS	
Signal Levels (Standard TTL)	0.0 to +0.4 V equals logic low +2.4 to Vcc equals logic high
Termination	All lines exceeding 2 feet will terminate with 220 ohm pull up resistors and 333 ohm pull down resistors
ENVIRONMENTAL REQUIREMENTS	
Operating Temperature	$65^{o}F$ to $75^{o}F$ ($18^{o}C$ to $25^{o}C$)
Operating Humidity	40% to 60% non-condensation
Operating Elevation	-500 to 7,000 feet above sea level
Storage and Shipping Altitude	-500 to 30,000 feet above sea level

(This Page Left Intentionally Blank)

SECTION 2

INSTALLATION

A2.1 GENERAL DESCRIPTION

The installation procedures are explained in the System Manual and the MTCD installation. They are therefore not repeated here.

(This Page Left Intentionally Blank)

SECTION 3

MAINTENANCE

A3.1 GENERAL DESCRIPTION

Maintenance of the Controller is limited to replacement of the Controller itself. This section will explain the Controller function only as an aid to the Service Engineer in troubleshooting.

A Functional Block Diagram is shown in Figure A3-1.

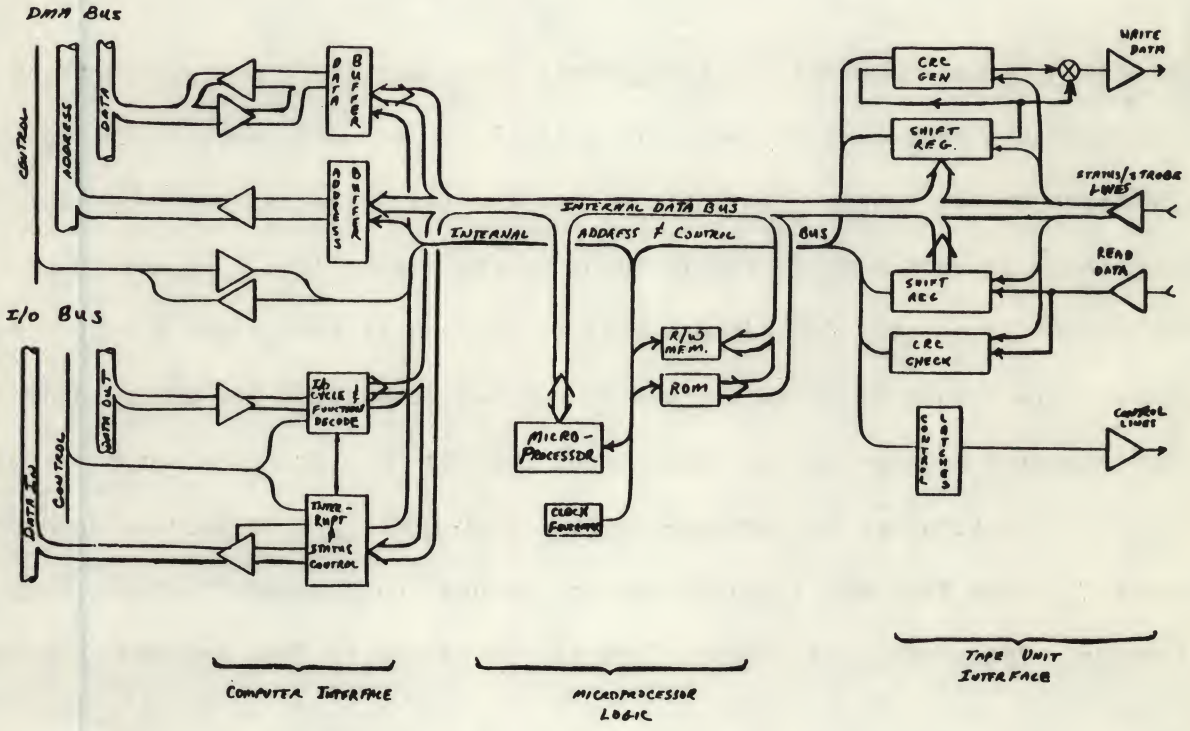


Figure A3-1. Cartridge Tape Controller Block Diagram

The Controller is a complete link between the computer program and the tape unit. The Controller performs command decoding, tape start/stop timing generation, tape record formatting, tape position, status reporting, and interrupt control. As such, it is a combination of Controller/Formatter.

The Controller is designed around a Z80 MOS Microprocessor. The three major functional (logic) blocks begin with the microprocessor logic.

A3.1.1 MICROPROCESSOR LOGIC

Memory addressing and I/O ranges are limited by design to be sufficient for use in this environment. The Microcomputer is comprised of the Z80, clock generator, buffers for Z80 address, and control line, memory bank, and I/O decoders.

The clock circuit divides the 5 megahertz CPU clock CPH2- by two, creating a 2.5 megahertz square wave clock. This clock is driven to most other clocked functions on the board. The buffers increase the drive capability of the Z80 outputs to drive the multiple TTL loads on the Controller. The memory bank decoder 6L translates Z80 address bits 9, 10, and 11 into eight 512 byte bank select lines. Since address lines 12 thru 15 are not connected, the memory address space consists of 4 kilobytes. By convention, the firmware for the Controller places this 4 kilobyte space in addresses 0000_{16} thru $OCFF_{16}$. The address decoder is enabled by the Z80 MREQ signal, creating unique "chip enable" outputs from the decoder. These select lines are directly connected to PROM and RAM chip enable pins.

The two I/O decoders (6D, 8F) are similar in their implementation. Both are enabled by the Z80 IØ and address bit 5. They are selectively enabled by the WR (write) and RD (read) control lines. They decode the three LSB address lines. Because address bit 5 is an enable, the decoders are active for IØ ports with addresses XXIXXyyy where X can be 0 or 1 and yyy is a 3 bit code.

So, for each yyy there are XXXX (16) possible occurrences. By firmware conventions the XXXX is always set to 0000, so the I/O decoders actually decode ports 20_{16} thru 27_{16}. Due to the timing relationship of the address lines and the IO-, RD-, and WR- control lines, the decoder outputs are "glitch-free" pulses. This is important as it allows the decoder outputs to be directly connected to the flip-flop clock and clear pins.

The Read/Write Memory's (RWM) and Read Only Memory's are 256 x 4 bit and 512 x 8 bit parts, respectively. The two RWM chips are enabled together to provide a 256 byte Read/Write Memory array (Note that 246 bytes of the "space" enable by MBK6- are unused). Each prom chip is uniquely enabled by one memory decode signal. The Controller has sockets for 6 ROM's, the seventh decode (MBK7-) is unused. The six sockets may not all be used, depending on the size of the firmware package.

Finally, the Data Bus Buffers created a high-fanout bidirectional bus from the 1-TTL-load drive of the Z80. (Note that the Read/Write Memories (which are very low-fanin MOS parts) connect to the actual Z80 bus.) All other parts are connected to the high-fanout bus.

The following tasks are performed by microprocessor logic:

1. Decode of all commands.
2. Monitoring and posting tape unit status.
3. Generation of all tape unit control signals and timing.
4. Formatting of records written on tape.
5. Byte-by-byte control of data transfers.
6. Initiation of interrupts.

The detailed control for each of the Controller operations resides in read-only-memory-resident firmware routines. A minimal amount of Random Access Memory is provided for scratch pad use by the firmware.

A3.1.2 COMPUTER INTERFACE LOGIC

This is composed of two parts, Programmed I/O and Direct Memory Access (DMA).

Programmed I/O

The Programmed I/O logic is used to receive and latch commands from the Basic Four CPU (hereafter called CPU). It also holds and reports status to the CPU. It decodes and latches the Initial Program Load (IPL) bus cycle, and performs the external interrupt function to the CPU.

The Programmed I/O logic does not operate on commands and status in any way. It serves only as a holding function and provides the response time necessary to participate in the CPU bus cycles (which the Z80 cannot respond to directly). The content of the command and status data bytes is controlled entirely by Z80 firmware.

DMA

The DMA (Direct Memory Access) logic is again mostly passive. An incrementing address register holds the address in Basic Four computer memory. The address is established by Z80 firmware according to the operation being performed (control block fetching, data transfer, status transfers, etc.). There is no direct connection of the DMA logic to any Cartridge Tape Controller (CTC) function other than the microprocessor. Memory input and output data is also handled passively. The DMA logic merely contains latches to hold the data. Data is always provided by or received by the Z80 firmware. The DMA logic in no way assigns any significance to either data or address.

The active portion of the DMA logic is the DMA control. This logic participates in all memory transfers, providing control signals, enabling address, and data is in proper timing sequence for operation with a BFC memory module.

Logic is included to allow the CTC to be placed in a DMA priority daisy chain; this enables the CTC to perform byte interweaving of DMA operations with other controllers equipped with this daisy chain logic.

Logic is included to decode bus cycles and perform the following bus operations:

1. Command and main status transmission over I/O bus.
2. Data, control, and auxiliary status input and output over DMA channel.
3. External interrupts.

A3.1.3 MAGNETIC TAPE (MTCD) INTERFACE LOGIC

The MTCD interface hardware includes logic for performing byte data transfers with the microprocessor and converting them to serial data transfers with the MTCD. The microprocessor does not deal with the bit-to-bit timing details of the MTCD data transfers.

A set of individually settable/resettable discrete latches is provided to supply control signals to the MTCD. The microprocessor firmware has direct control over these control lines. Thus, all the details of MTCD control timing and sequence (i.e., the tape formatting/positioning functions) is resident in Z80 firmware. The control logic in the MTCD interface is, therefore, mainly passive.

MTCD status is routed through a set of latches that allow the firmware to read it. The MTCD hardware does not react to MTCD status or status changes there are minor exceptions to this which will be discussed in the detailed description of the logic).

The data handling portion of the MTCD interface logic consists of the following functions:

1. A shift register for parallel-to-serial and serial-to-parallel conversion.
2. Bit counters to define 8-bit byte increments of data.

3. CRC generation and checking logic.

4. Logic to synchronize tape unit strobes and data to internal CTC timing.

5. Z80 interrupt logic for read-after-write control and escape from tape unit hang-up situations.

This functional block contains the line drivers and receivers, data buffer registers and the decode logic necessary for the microprocessor to control the tape unit(s). Hardware for read and write CRC calculations is included.

A3.2 FUNCTIONAL PARAMETERS

Data reliability of the Controller is subject to the limits of the MTCD.

Soft Error Rate (Recoverable Errors) is not more than one error in 10^8 bits of data transferred.

SECTION 4

RECOMMENDED SPARE PARTS/GLOSSARY

A4.1 RECOMMENDED SPARE PARTS LIST

TABLE A4-1. SPARE PARTS

Item Number	BFC/MM Number	Vendor Part Number	Description	Quantity
1	B903030	610010	Controller, PCB	1
2	900960-002	610710	Cable	1

A4.2 GLOSSARY OF MNEMONICS

MNEMONIC	MEANING
AC	Abnormal Condition. This bit amplifies the FP, CRC and EOT bits. When set in conjunction with FP, AC indicates a write command was issued to a File Protected Unit, the command is aborted. When set in conjunction with EOT, AC indicates tape has reached physical End of Tape (EOT). When set in conjunction with CRC, AC indicates a data dropout has occurred during a Read or Write Command. The last command has therefore reached an unpredictable conclusion. AC will be set if the Not Ready, Device Busy, or Illegal Command situations occur. These conditions are reflected in the Auxiliary Status byte. AC will also be set if a Read, Read Format, or Write Command is issued with a DMA Byte count of 0 in the Control Block.
BF	Busy Flag. This bit allows the Controller to be run in an interrupt-drive environment or a test flag environment. When busy, the Controller will set the Busy Flag. If the Busy Flag is set, the software should not issue any commands to the Controller. The Controller will reset BF when it is again ready to accept a new command. NOTE: The Controller can take up to 500 microseconds to set the Busy Flag after a command has been received.
BOT	The tape in the cartridge is positioned at the Beginning of Tape (BOT).

MNEMONIC	MEANING
CC	1 - Command Complete Interrupt 0 - Attention Interrupt
CRC	This bit is set if during a read or read-after-write operation, a CRC error is detected.
EOT	The tape in the cartridge is positioned in the End of Tape (EOT) warning area or is physically the EOT. This latter condition is undesirable. When it occurs, bit 0 (AC) is also set.
FM	File Mark. This bit is set after a Write File Mark command or after a Read or Space command that terminates immediately after traversing a File Mark record.
FP	The tape unit is loaded with a cartridge that is file protected (refer also to AC).

AUXILIARY STATUS BYTE

MNEMONIC	MEANING
DB	Device Busy. The desired unit is busy rewinding.
IC	Illegal Command Code.
NR	Not Ready. The desired tape unit is not ready for one or more of the following reasons: 1. Power (+5 volts dc) not applied to the unit. 2. No cartridge installed. 3. The BOT/EOT sensor lamp is burned out.
T	When set, indicates that the command just completed was performed in the test mode.
TR	Track Number. The binary coded number of the track selected during performance of the command. This will always agree to the TR field in the command, except that TR will always be 0 for a rewind termination.
#	Unit Number. The number of the unit or test associated with the interrupt.

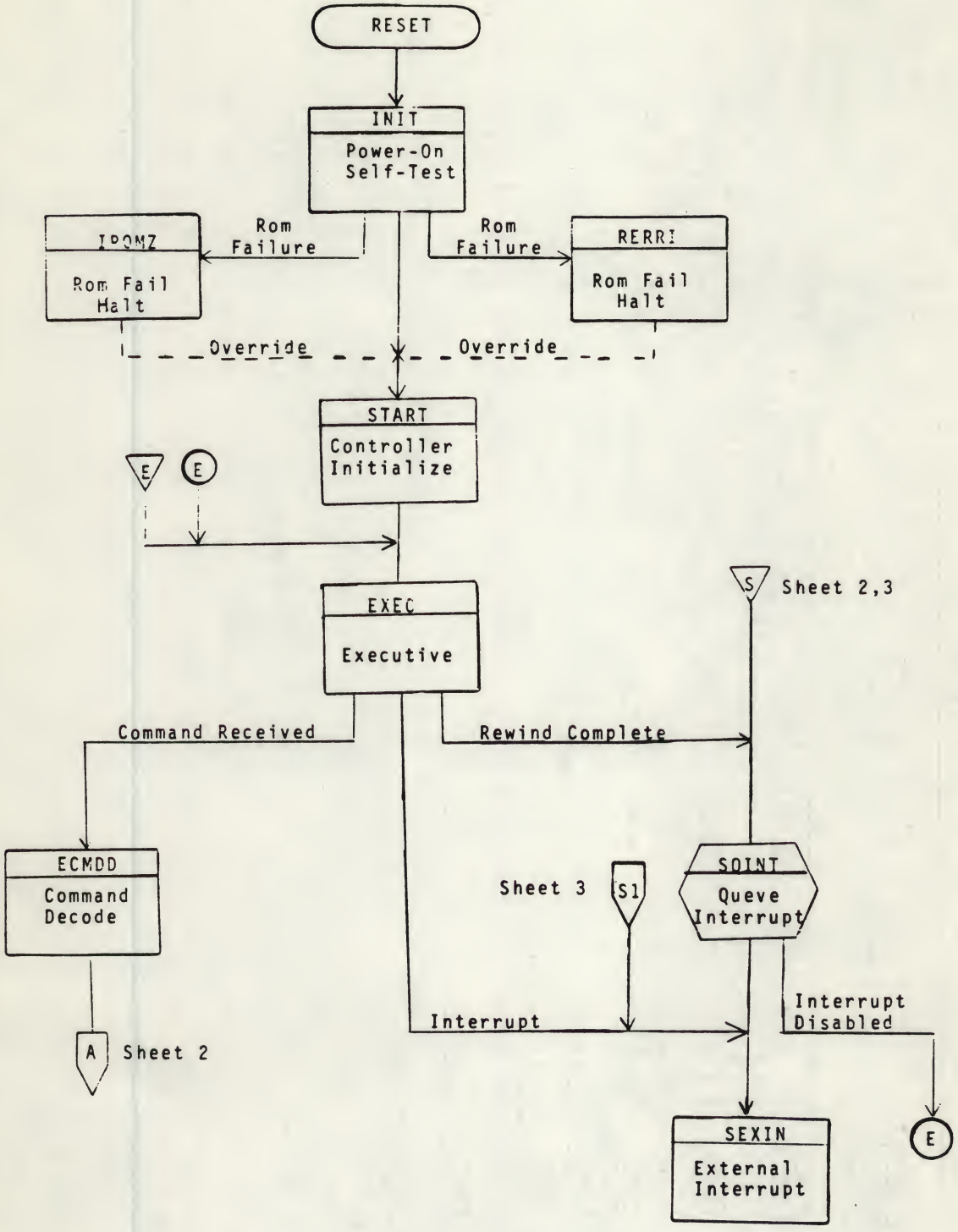
SECTION 5

REFERENCE DATA

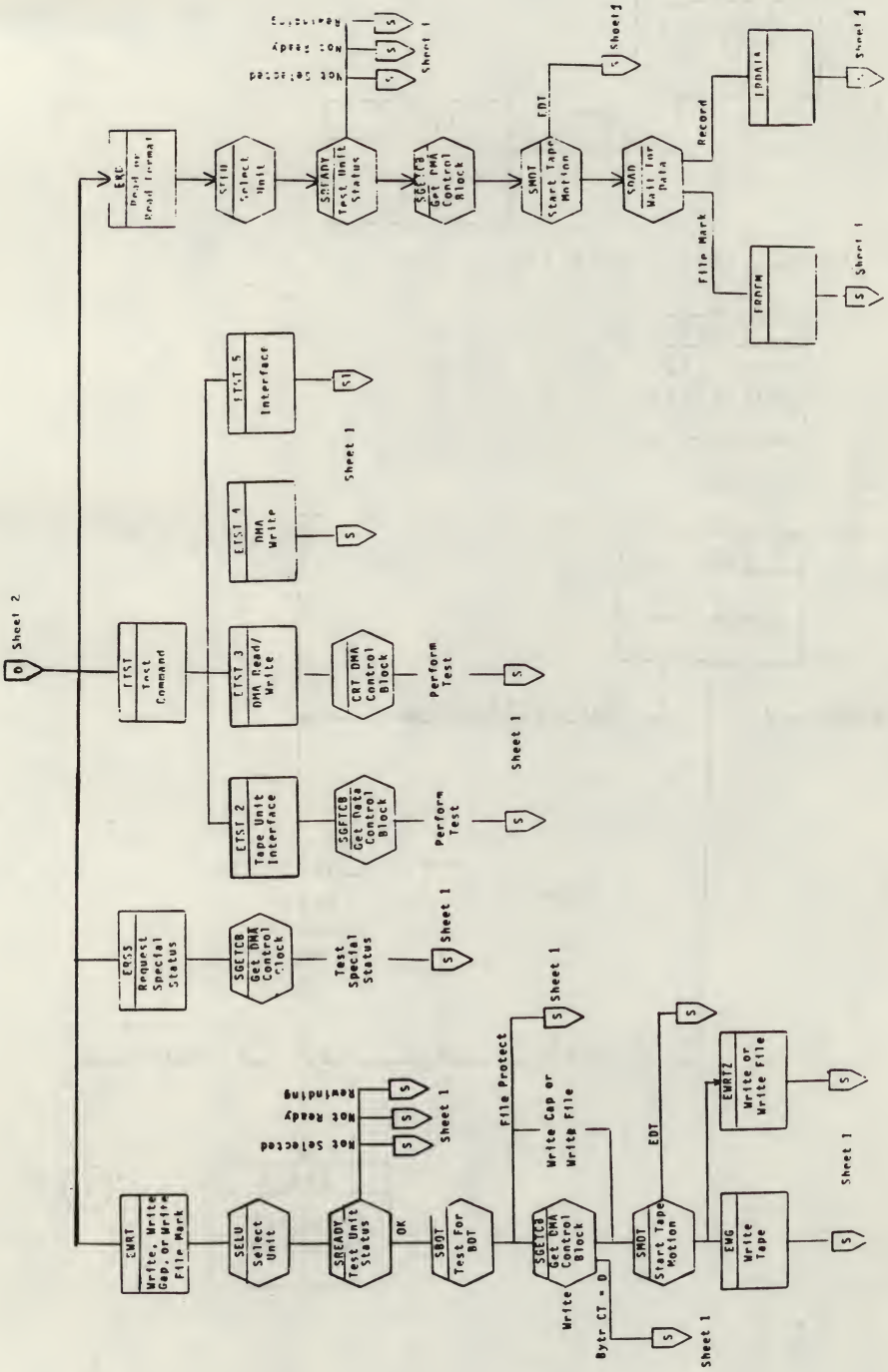
5.1 REFERENCE DATA

Major Flow Diagrams

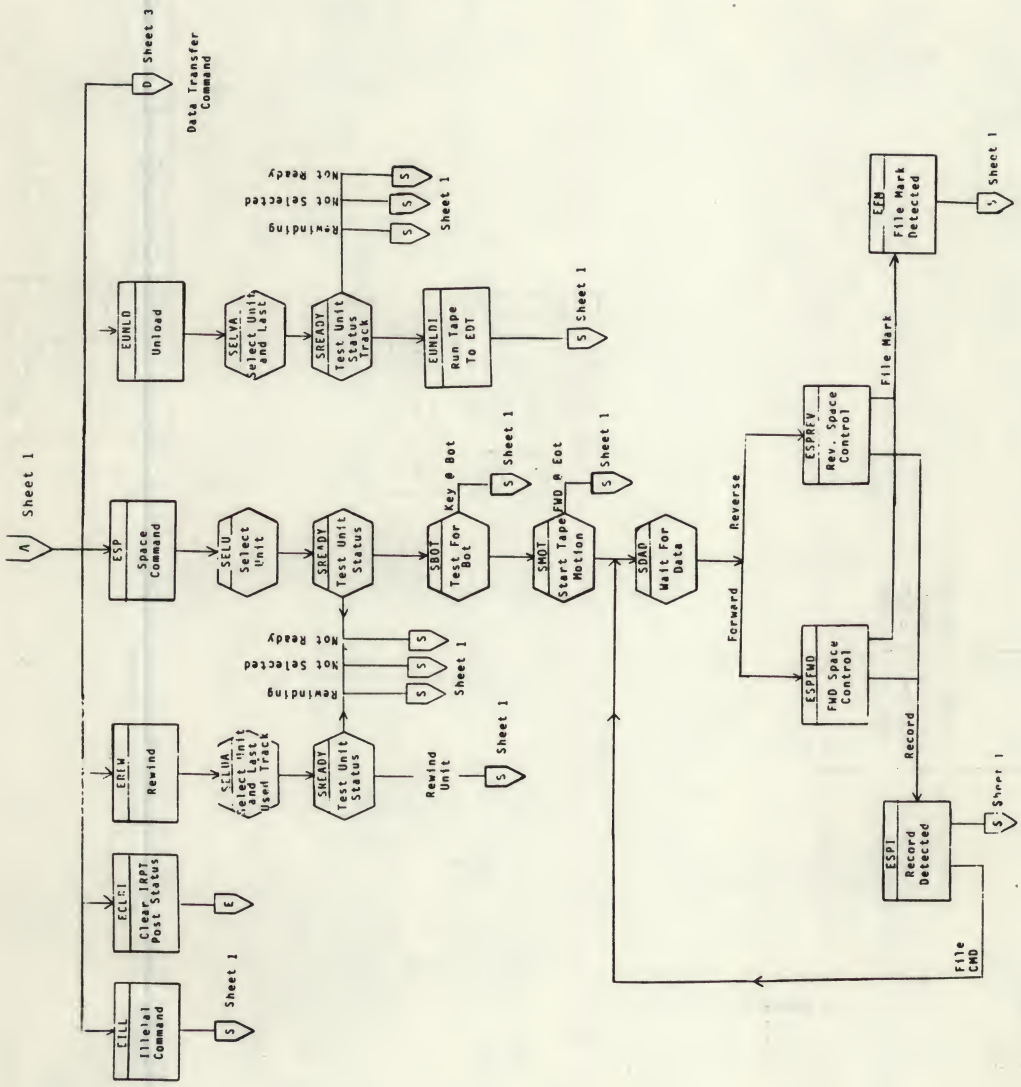
Sheet	Contents
1 of 3	Control Structure
2 of 3	Non-Data-Transfer Commands
3 of 3	Data Transfer Commands



Control Structure (Sheet 1 of 3)

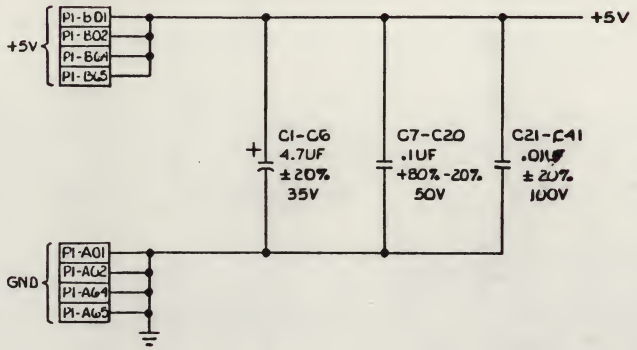


Data Transfer Commands (Sheet 3 of 3)



Non-Data Transfer Commands (Sheet 2 of 3)

REVISION BLOCK				
REV LTR	ER ECN	DESCRIPTION	MATERIAL	DATE
AX1	1870	[illegible]	[illegible]	[illegible]
AX2	1924	SEE ECN	[illegible]	[illegible]
AX3	[illegible]	SEE ECN [illegible]	[illegible]	[illegible]
H	2343	PRODUCTION RELEASE	1.1	4-17-78
B	2519	CHANGED LOGIC SHTS. 2, 13 & 14	1.1	6-14-78
C	2541	CHANGED LOGIC SHTS. 1, 2, 8 & 10	1.1	8-3-78



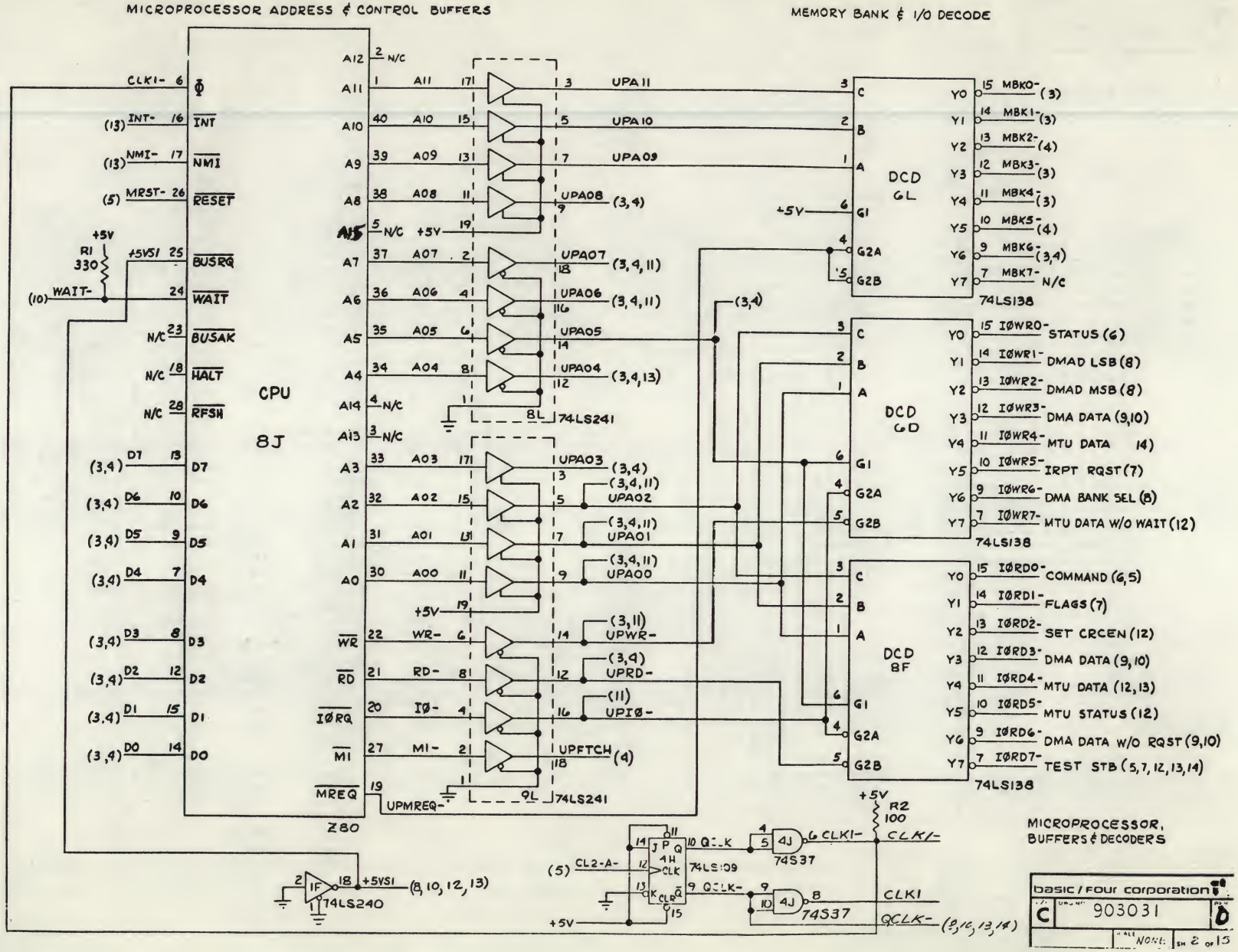
UNUSED GATES		
LOC	COML. NO.	NO.
6B	74LS68	1
5L	74LS00	1
6E	74LS04	1
4L	74LS20	1
1E	7438	1
5K	7438	1
1F	74S240 *	3
8C	74S240 *	2

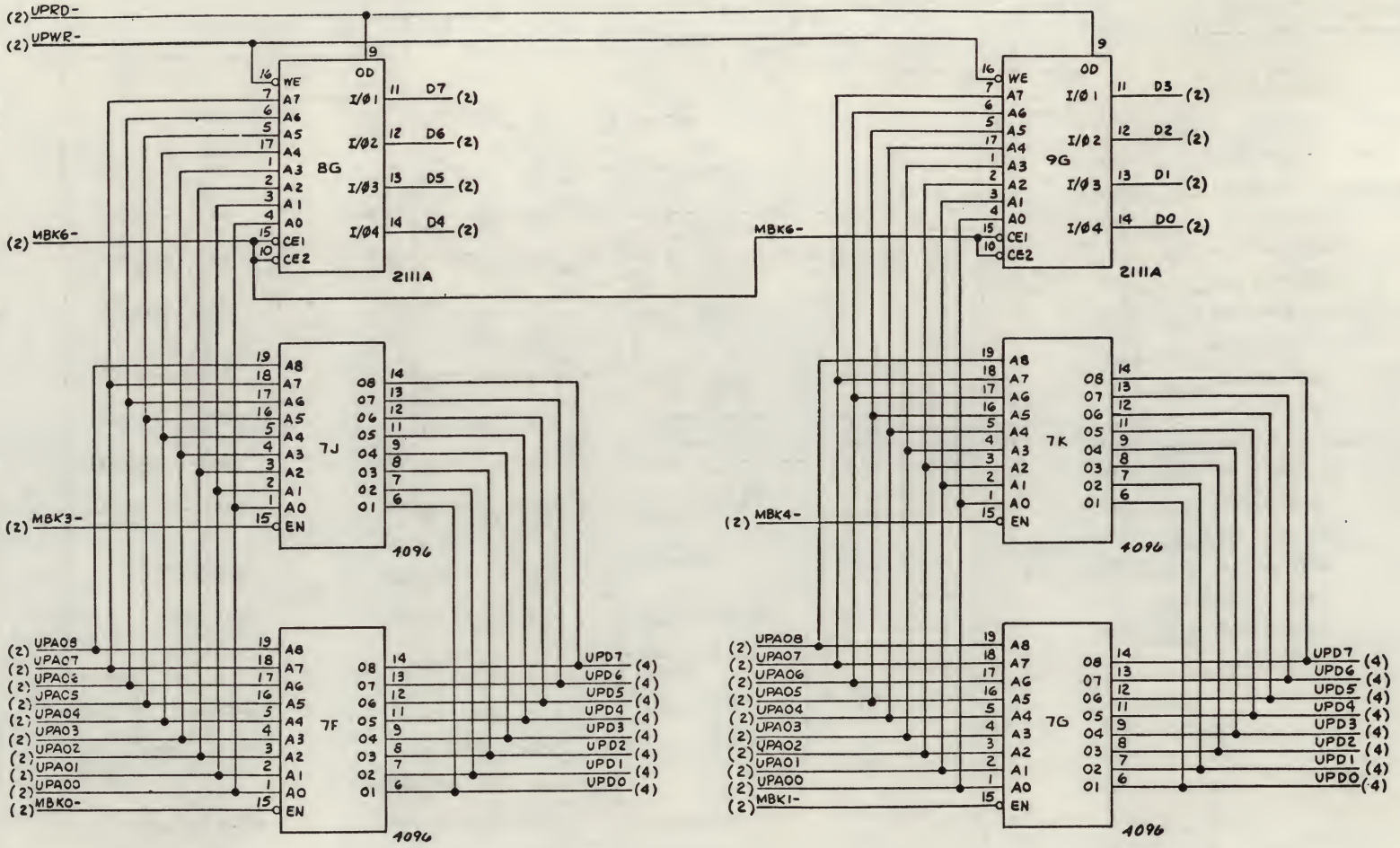
* CONTROL LINES TIED TO GND

3. FOR P1 AND P2 CONNECTOR FUNCTIONS SEE SHT 15
2. I.C. DESIGNATIONS ON F/D INDICATE BOARD LOCATION. FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH "U". EXAMPLE: "U6A".
1. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 WATT.

NOTES UNLESS OTHERWISE SPECIFIED

		DIMENSIONS ARE IN INCHES TOLERANCES UNLESS OTHERWISE SPECIFIED X ± 1 XX ± 03 XXX ± 010 ANGLES ± 1.0° MACHINED SURFACES √	basic / four corporation 1335 South Claudina Street Anaheim, California 92805			
				DRAWN	K.G. NANCE	6-29-77
				CHKD	[illegible]	9-22-77
				ENG	D. Anderson	9-23-77
				MFG		
[illegible]	INF			APP	K.C. [illegible]	9-27-77
NEXT ASSY	USED ON	DO NOT SCALE DRAWING	TITLE LD CARTRIDGE TAPE CONT			
			SIZE C	DWG NO 903031	REV D	
			SCALE NONE	SH 1 OF 15		


MICROPROCESSOR ADDRESS & CONTROL BUFFERS
MEMORY BANK & I/O DECODE
CPU
8J
Z80
CLK1-
INT-
NMI-
MRST-
BUSRQ
WAIT-
BUSAK
HALT
RFSH
D7
D6
D5
D4
D3
D2
D1
D0
WR
RD
IØRQ
MI
MREQ
UPMREQ-
UPA11
UPA10
UPA09
UPA08
UPA07
UPA06
UPA05
UPA04
UPA03
UPA02
UPA01
UPA00
UPWR-
UPRD-
UPIØ-
UPFETCH
74LS241
8L
9L
74LS138
DCD 6L
DCD 6D
DCD 8F
MBK0-
MBK1-
MBK2-
MBK3-
MBK4-
MBK5-
MBK6-
MBK7-
IØWR0-
IØWR1-
IØWR2-
IØWR3-
IØWR4-
IØWR5-
IØWR6-
IØWR7-
IØRD0-
IØRD1-
IØRD2-
IØRD3-
IØRD4-
IØRD5-
IØRD6-
IØRD7-
STATUS (6)
DMAD LSB (8)
DMAD MSB (8)
DMA DATA (9,10)
MTU DATA 14)
IRPT RQST (7)
DMA BANK SEL (8)
MTU DATA W/O WAIT (12)
COMMAND (6,5)
FLAGS (7)
SET CRCEN (12)
DMA DATA (9,10)
MTU DATA (12,13)
MTU STATUS (12)
DMA DATA W/O RQST (9,10)
TEST STB (5,7,12,13,14)
74LS240
74LS109
74S37
CL2-A-
CLK1-
CLK1
QCLK-
R1 330
R2 100
+5V
+5VSI
MICROPROCESSOR, BUFFERS & DECODERS
basic/four corporation
903031
SH 2 OF 15

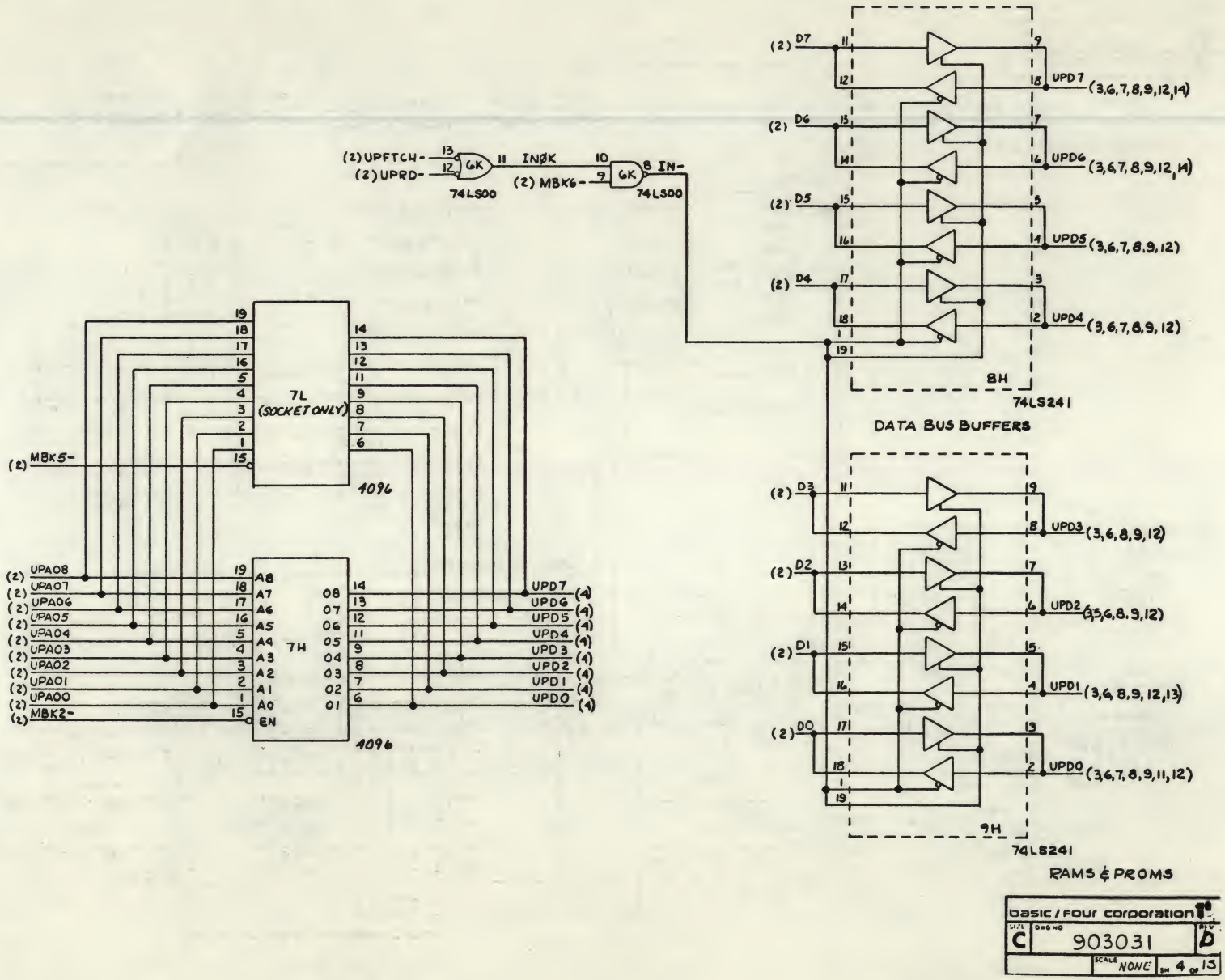


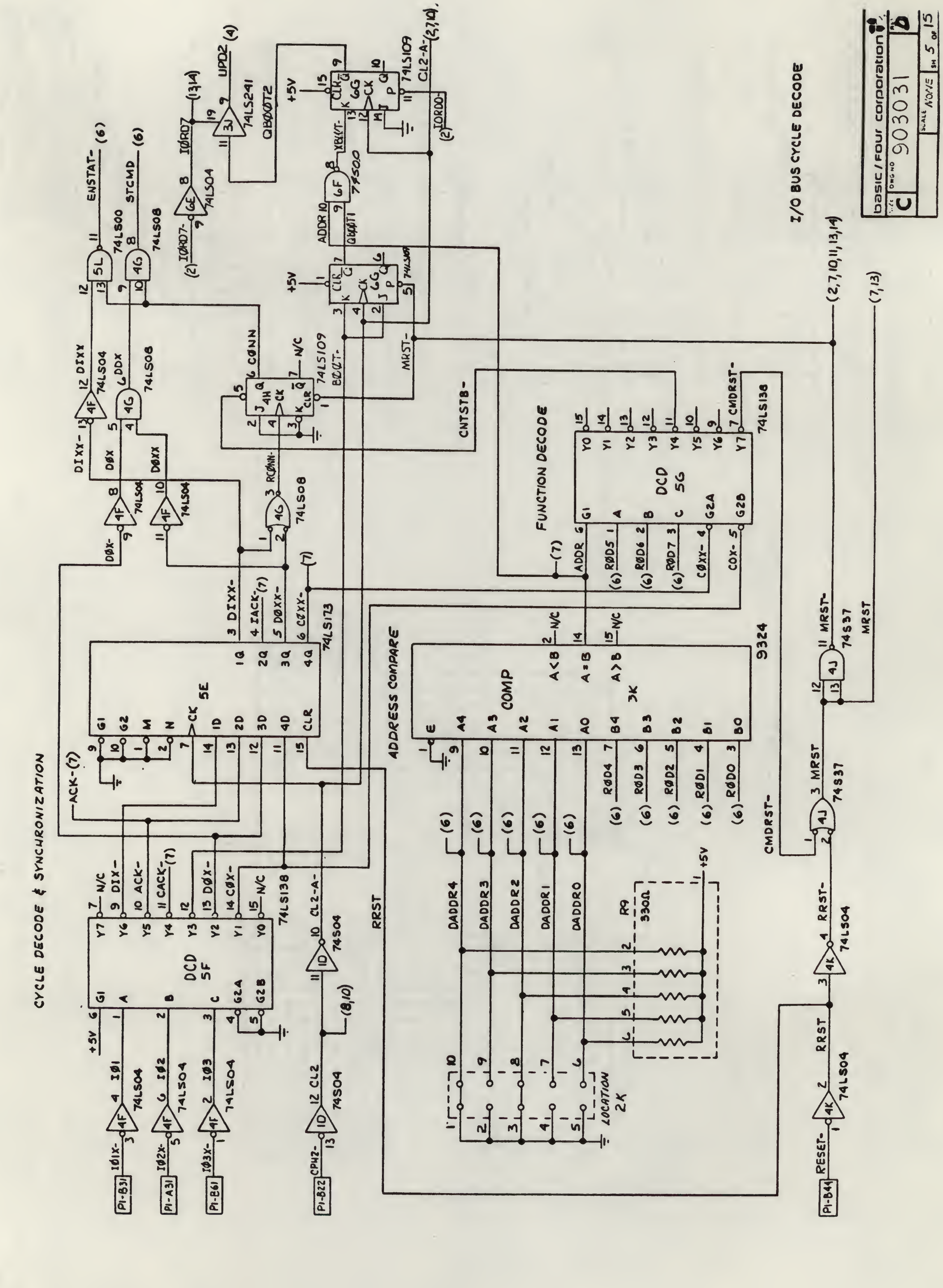
RAMS & PROMS

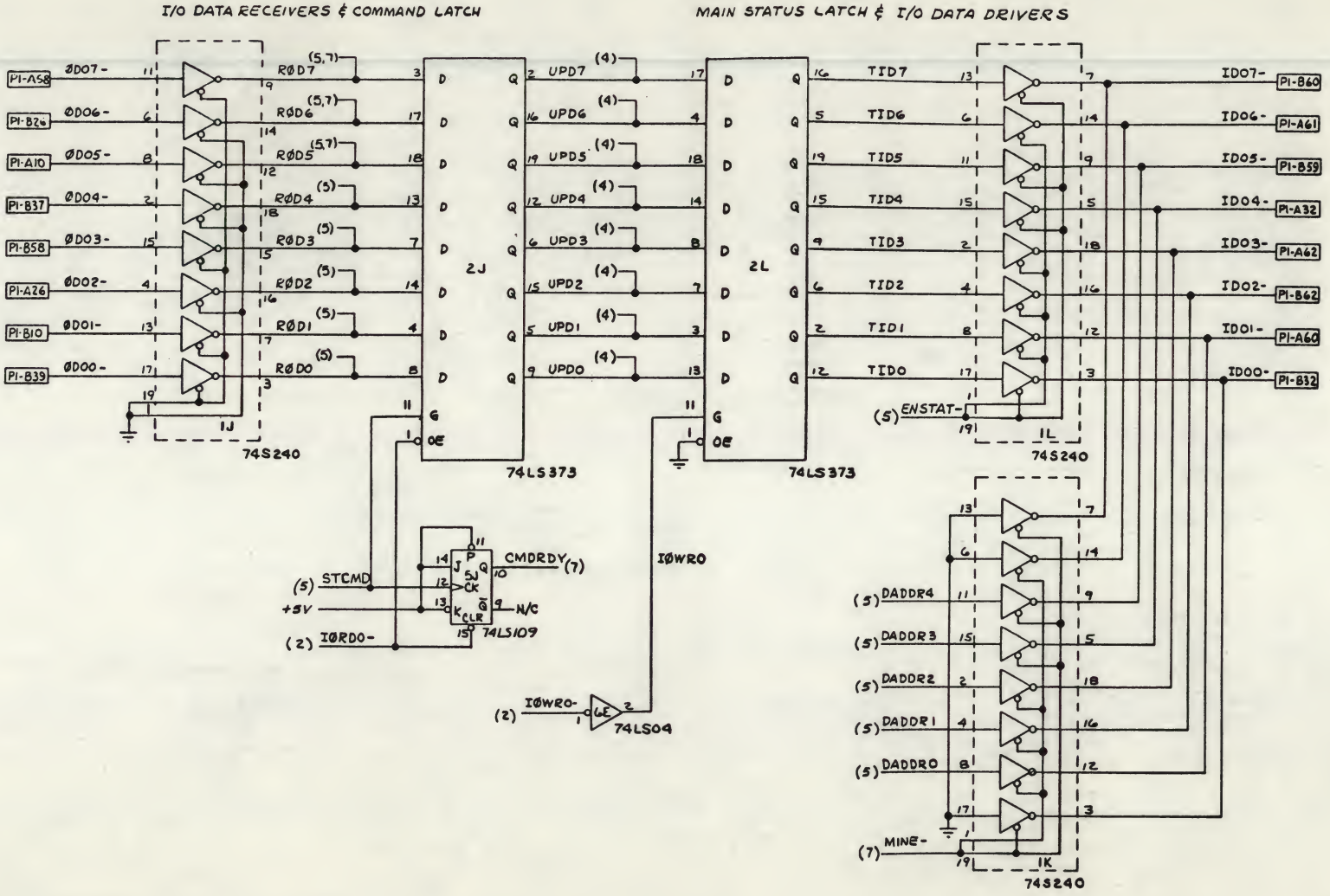
basic/four corporation

SIZE	DWG NO	REV
C	903031	D

SCALE NONE SH 3 OF 15


(2) UPFTCH-
(2) UPRD-
74LS00
INØK
(2) MBK6-
IN-
74LS00
(2) D7
(2) D6
(2) D5
(2) D4
UPD7 (3,6,7,8,9,12,14)
UPD6 (3,6,7,8,9,12,14)
UPD5 (3,6,7,8,9,12)
UPD4 (3,6,7,8,9,12)
8H
74LS241
DATA BUS BUFFERS
(2) D3
(2) D2
(2) D1
(2) D0
UPD3 (3,6,8,9,12)
UPD2 (3,5,6,8,9,12)
UPD1 (3,6,8,9,12,13)
UPD0 (3,6,7,8,9,11,12)
9H
74LS241
RAMS & PROMS
7L
(SOCKET ONLY)
4096
(2) MBK5-
7H
4096
(2) UPA08
(2) UPA07
(2) UPA06
(2) UPA05
(2) UPA04
(2) UPA03
(2) UPA02
(2) UPA01
(2) UPA00
(2) MBK2-
UPD7 (4)
UPD6 (4)
UPD5 (4)
UPD4 (4)
UPD3 (4)
UPD2 (4)
UPD1 (4)
UPD0 (4)
basic/four corporation
C
903031
D
SCALE NONE
SH 4 OF 13

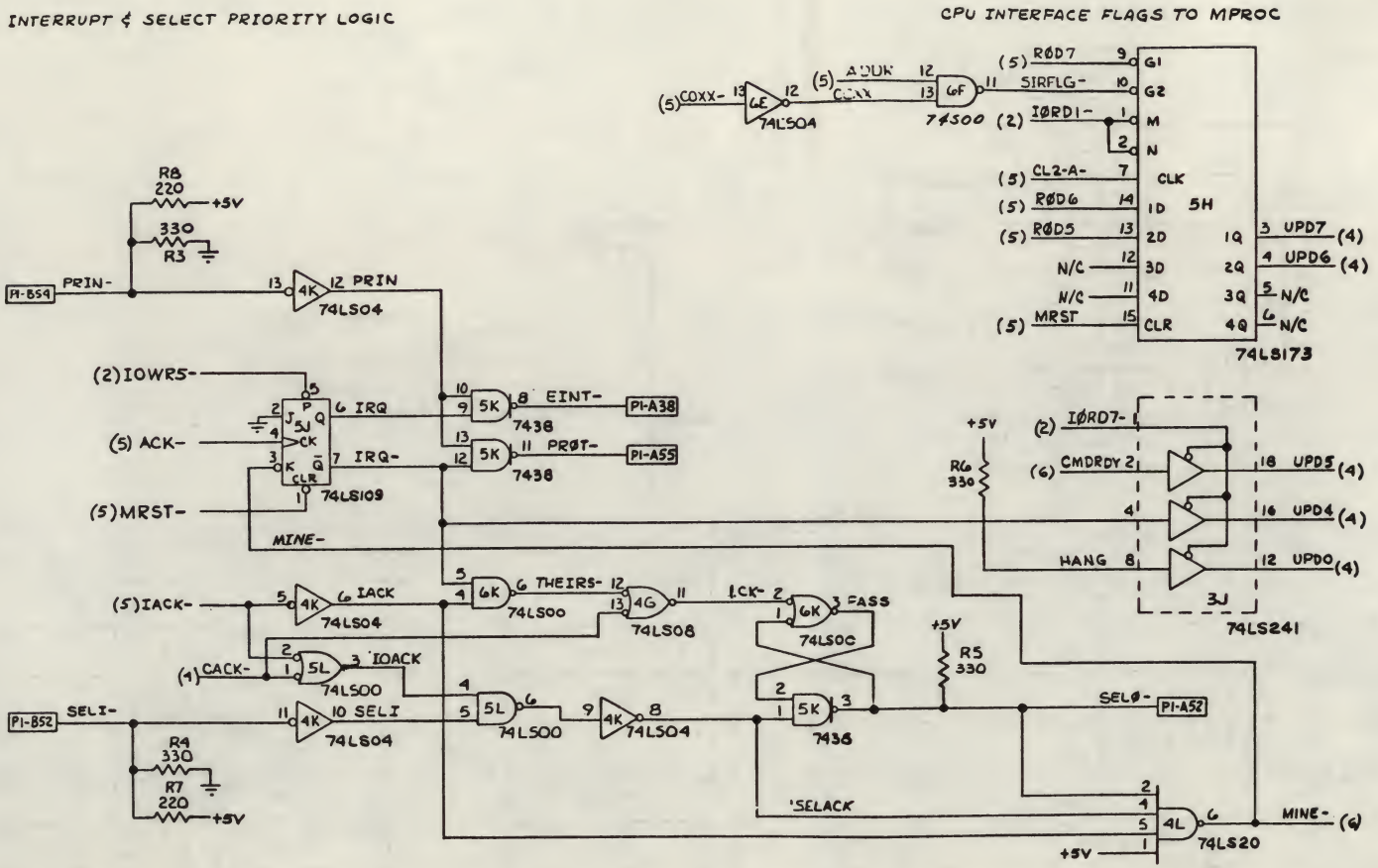

CYCLE DECODE & SYNCHRONIZATION
ADDRESS COMPARE
FUNCTION DECODE
I/O BUS CYCLE DECODE
basic/four corporation
C
903031
NONE
5 of 15



I/O BUS COMMAND & STATUS

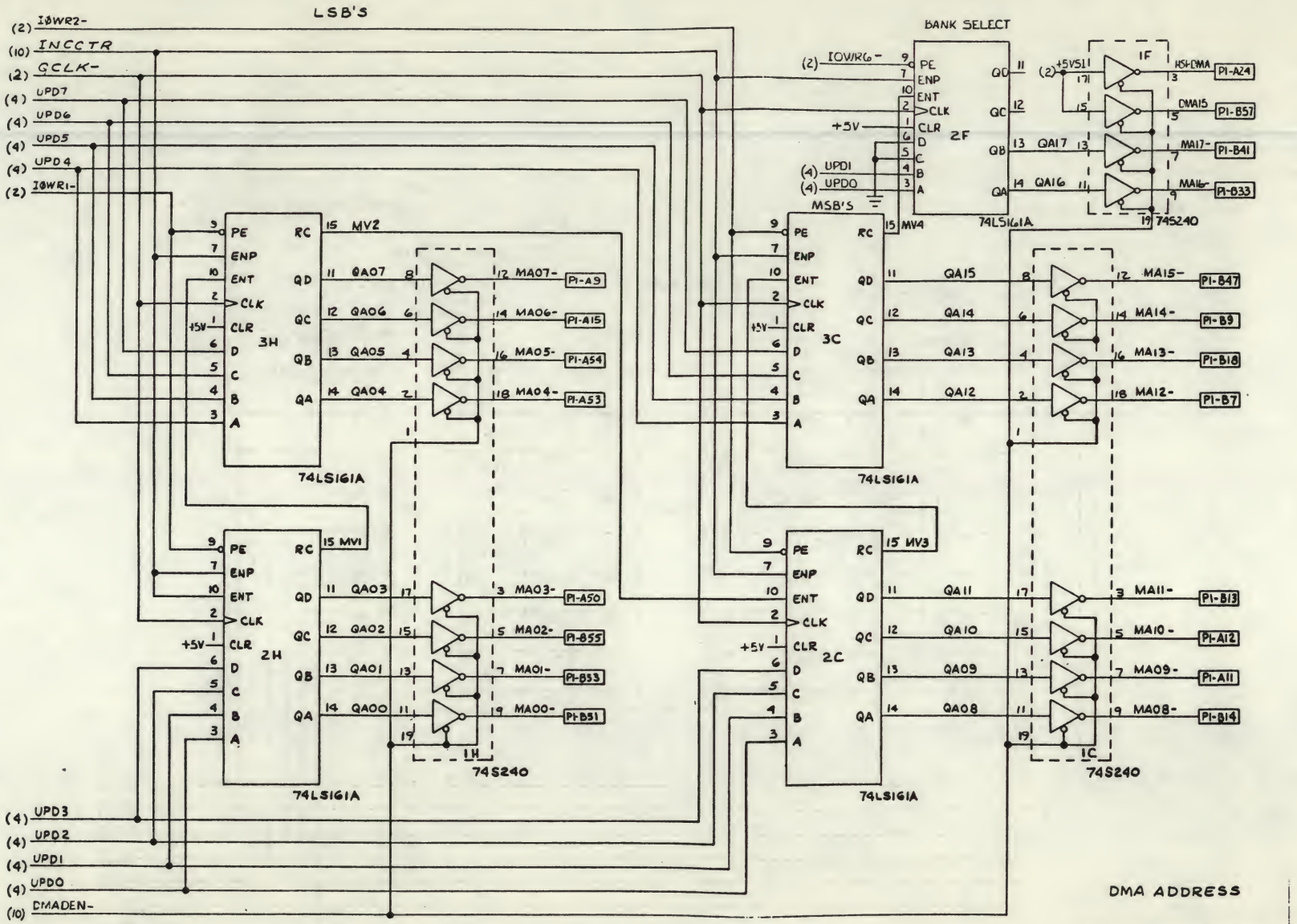
basic/four corporation

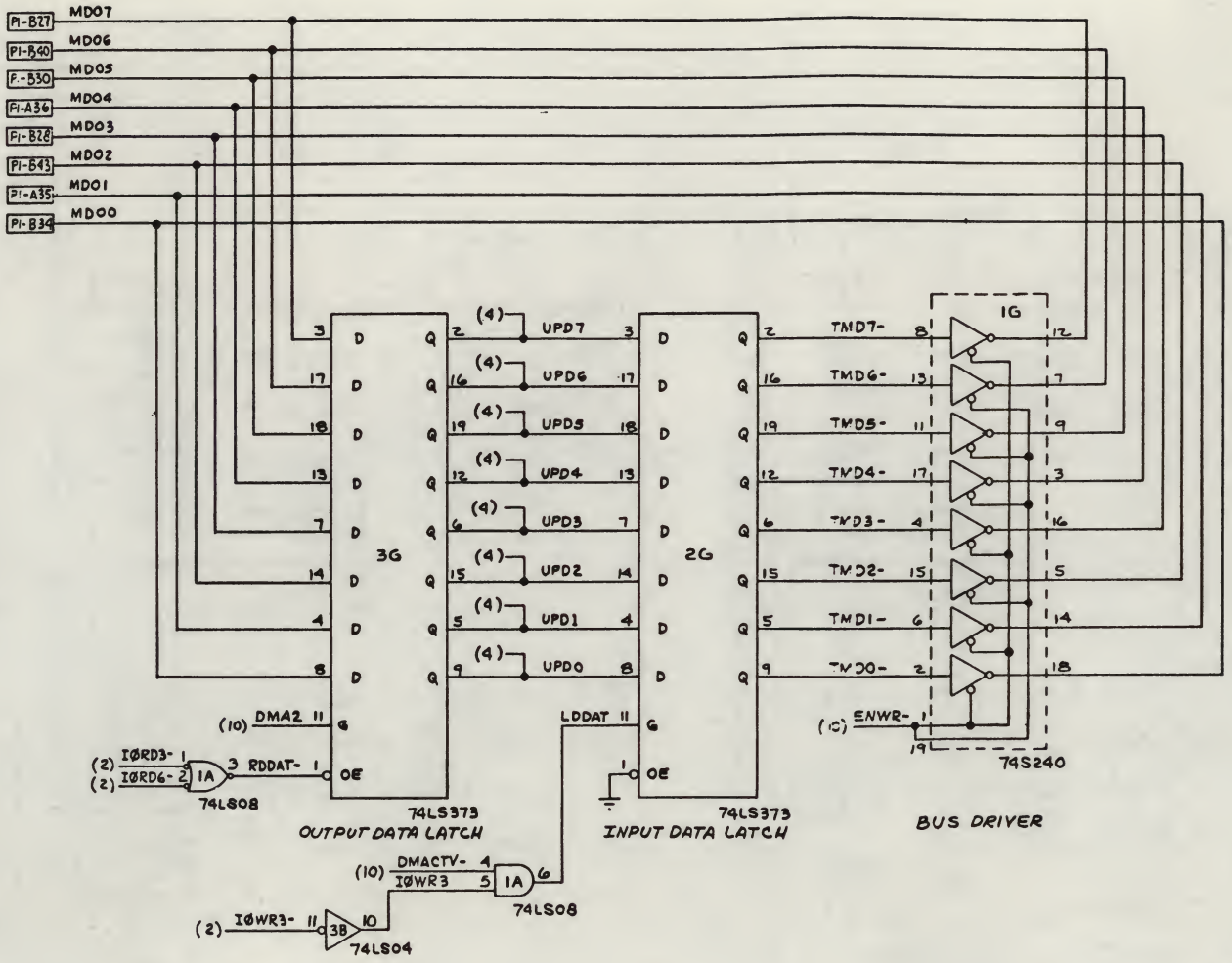
SIZE	DRG NO	REV
C	903031	D
SCALE NONE	SH 6 OF 15	



basic/four corporation

SIZE	DWG NO	REV
C	903031	D
	SCALE NONE	SH 7 OF 15

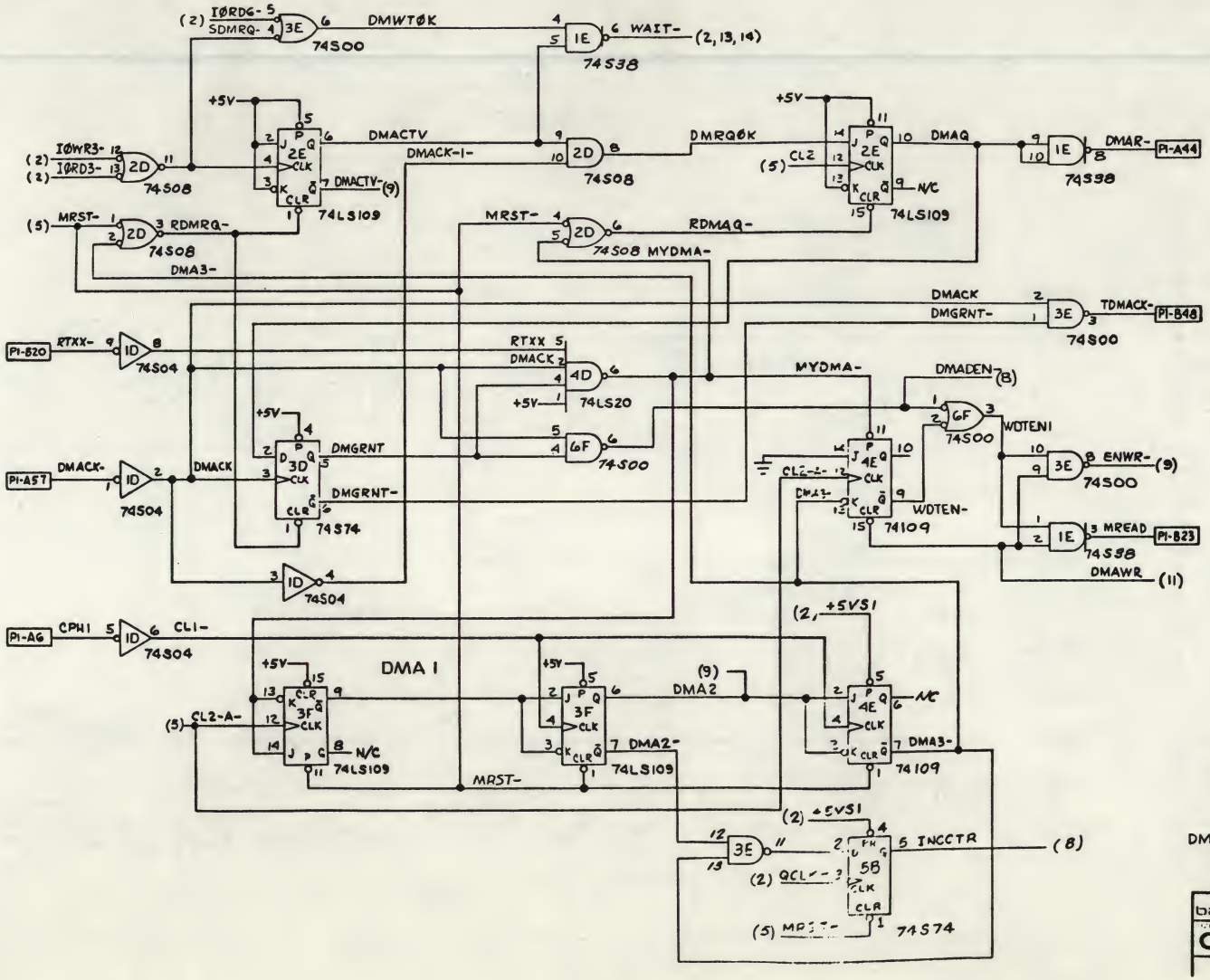

LSB'S
BANK SELECT
MSB'S
(2) IOWR2-
(10) INCCTR
(2) GCLK-
(4) UPD7
(4) UPD6
(4) UPD5
(4) UPD4
(2) IOWR1-
(2) IOWR6-
+5V
(4) UPD1
(4) UPD0
2F
74LS161A
1F
74S240
MV2
MV1
MV4
MV3
3H
2H
3C
2C
1H
1C
74LS161A
74S240
QA07
QA06
QA05
QA04
QA03
QA02
QA01
QA00
QA15
QA14
QA13
QA12
QA11
QA10
QA09
QA08
QA17
QA16
MA07-
MA06-
MA05-
MA04-
MA03-
MA02-
MA01-
MA00-
MA15-
MA14-
MA13-
MA12-
MA11-
MA10-
MA09-
MA08-
MA17-
MA16-
DMA15
HSI-DMA
P1-A9
P1-A15
P1-A54
P1-A53
P1-A50
P1-B55
P1-B53
P1-B51
P1-B47
P1-B9
P1-B18
P1-B7
P1-B13
P1-A12
P1-A11
P1-B14
P1-B57
P1-B41
P1-B33
P1-A24
(4) UPD3
(4) UPD2
(4) UPD1
(4) UPD0
(10) DMADEN-
DMA ADDRESS
basic/four corporation
C
903031
D
SCALE NONE
SH 8 OF 15



DMA DATA

basic / four corporation

C	903031	0
SCALE NONE	SH 9 OF 15	

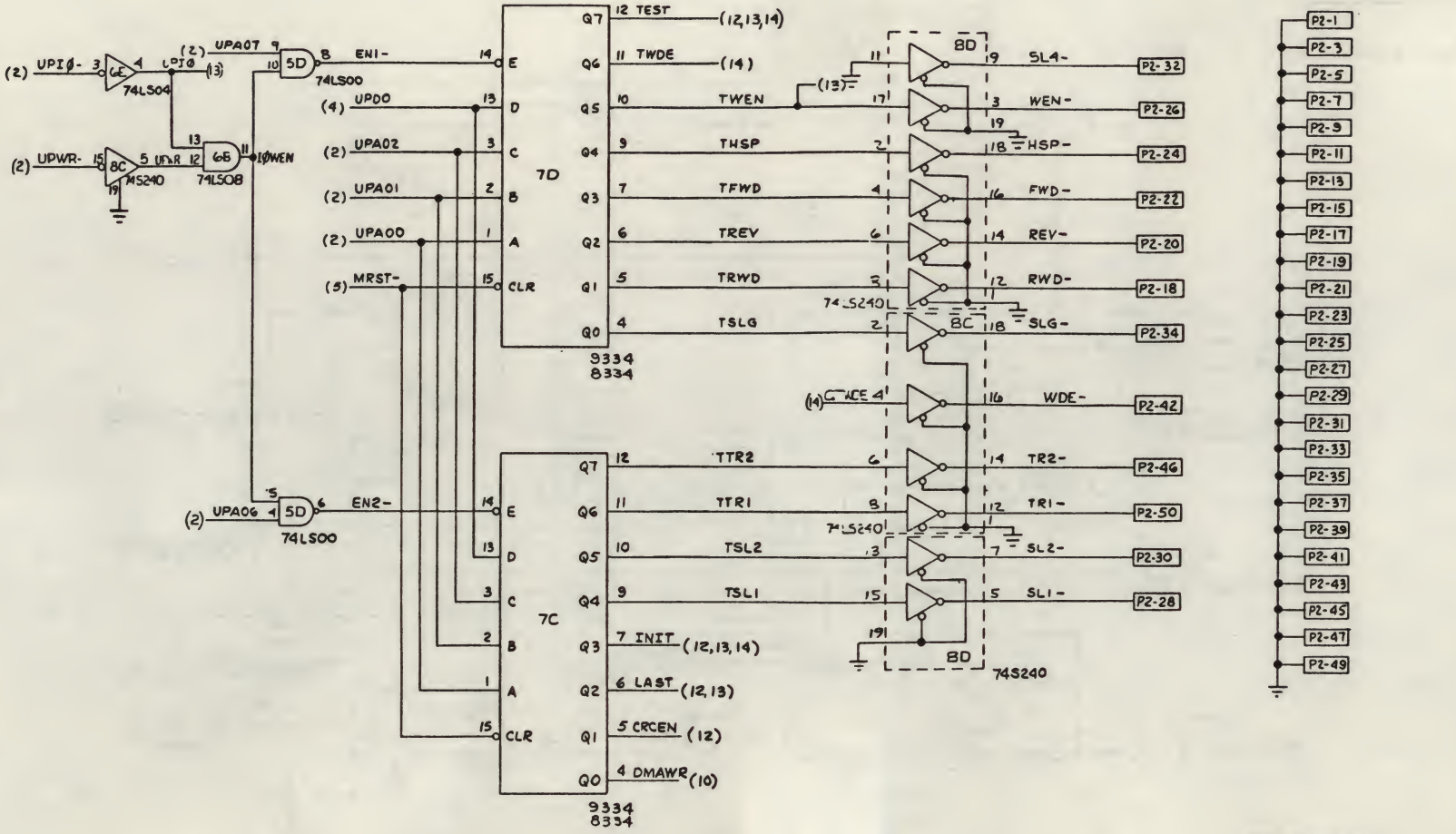


DMA CONTROL & PRIORITY

basic/four corporation

SIZE	DWG NO	REV
C	903031	D
	ALL NONE	SH 10 OF 15

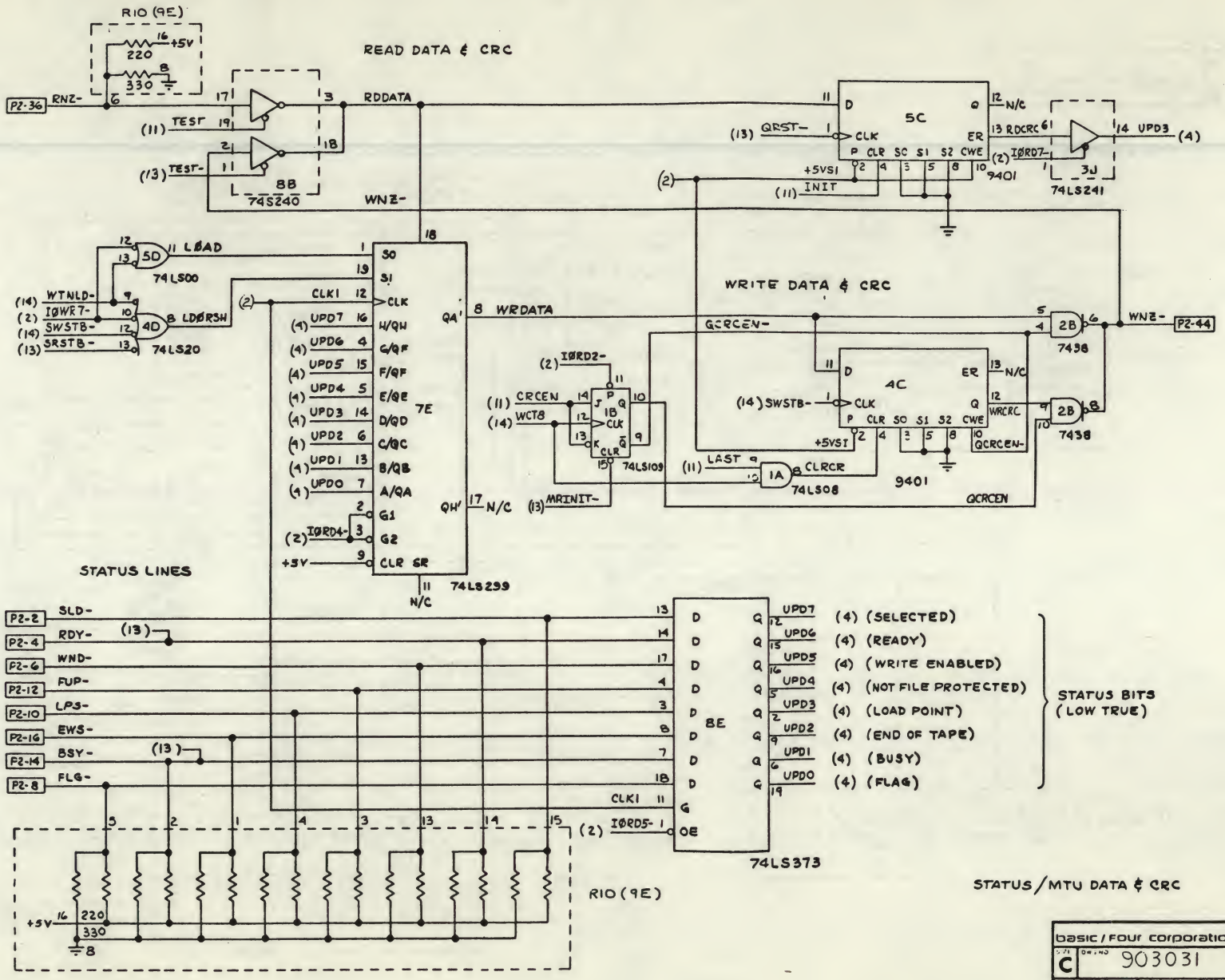
CONTROL LINES



MTU CONTROL

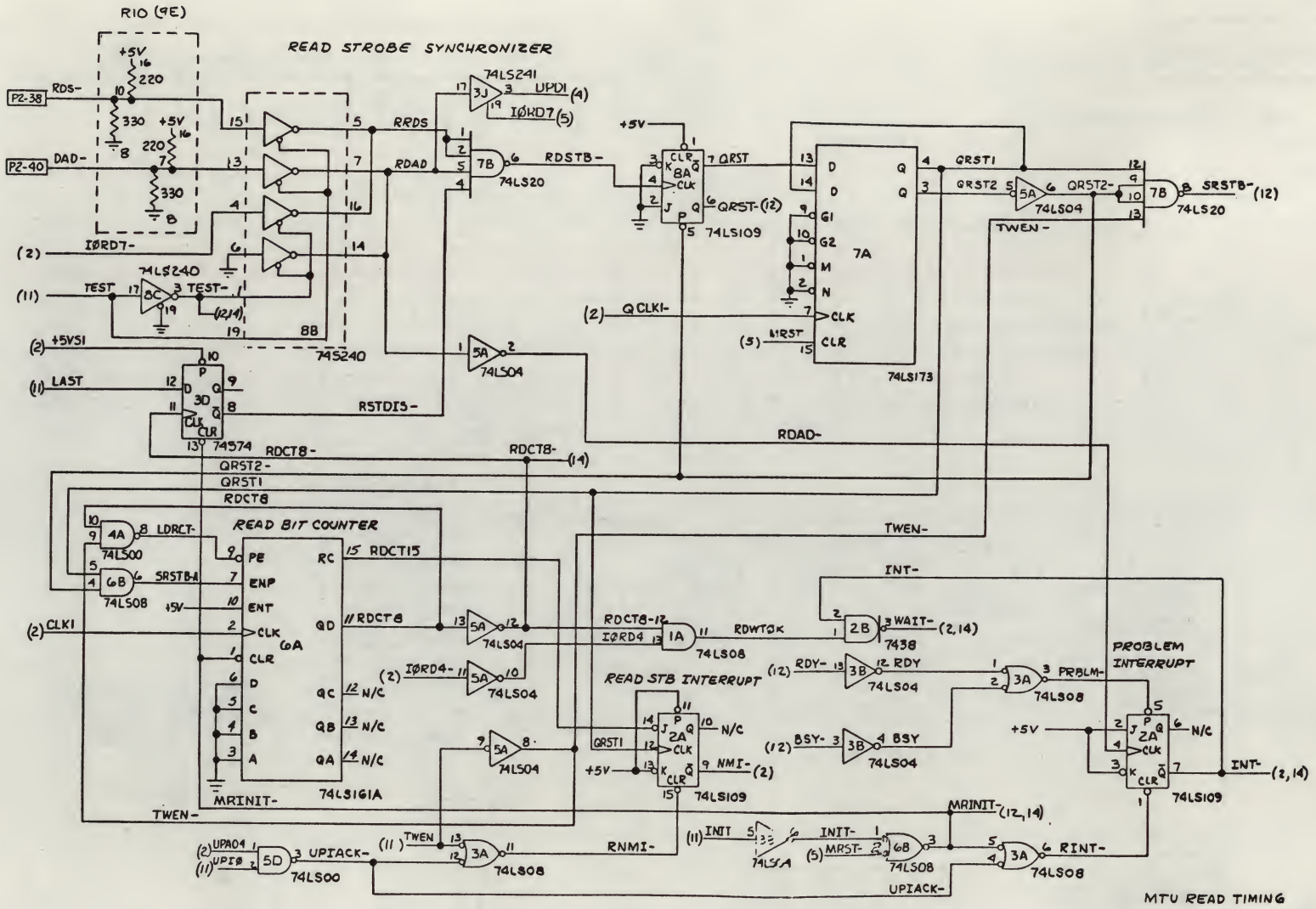
basic / four corporation

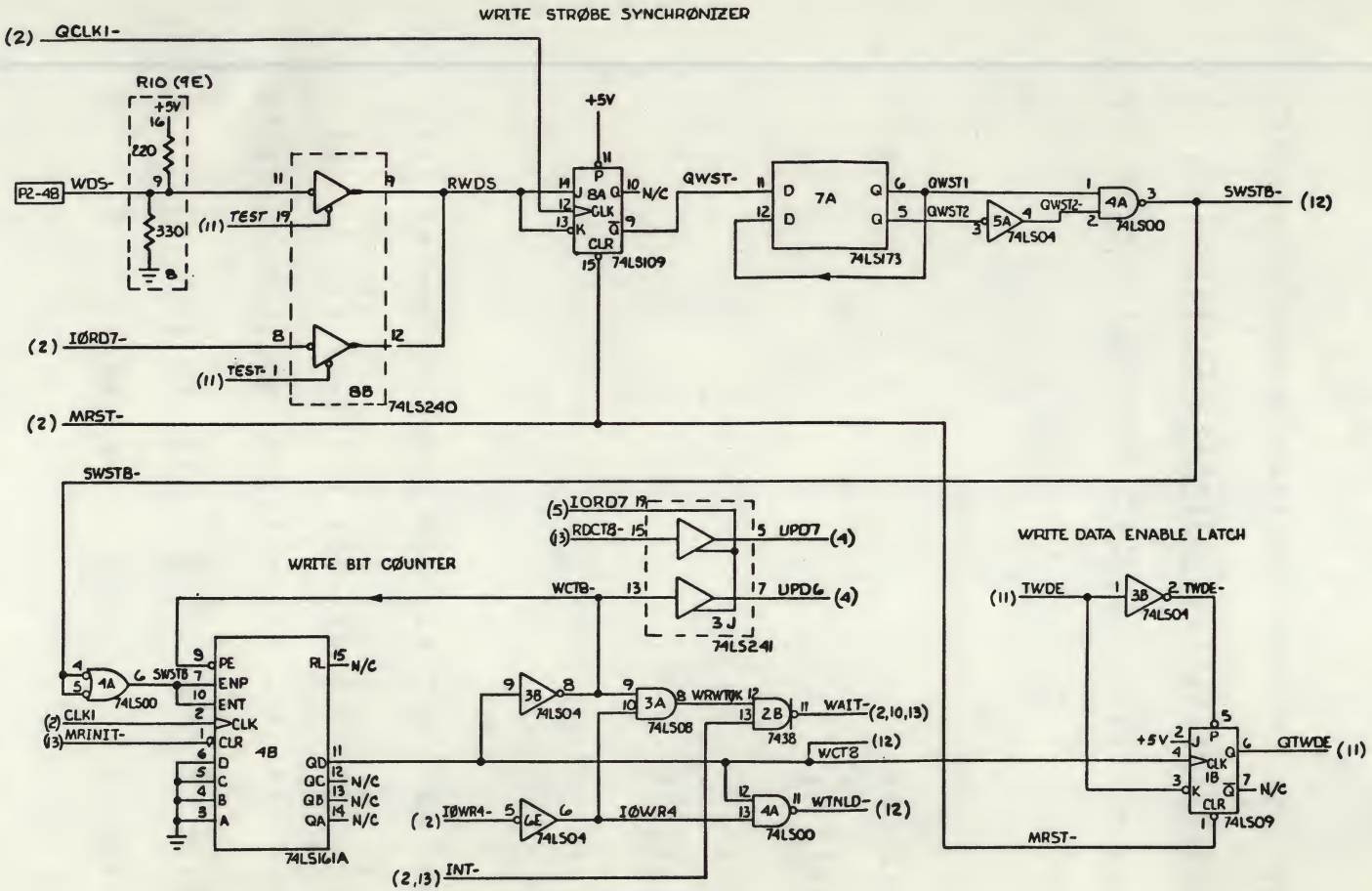
C	DWG NO 903031	REV D
	SCALE NONE	SH 11 OF 15



basic/four corporation

SIZE	DWG NO	REV
C	903031	D
	SCALE NONE	SH 12 OF 15


R10 (9E)
READ STROBE SYNCHRONIZER
READ BIT COUNTER
READ STB INTERRUPT
PROBLEM INTERRUPT
MTU READ TIMING
RDS-
DAD-
IØRD7-
TEST
TEST-
LAST
RSTDIS-
RDCT8-
QRST2-
QRST1
RDCT8
TWEN-
INT-
MRINIT-
RNMI-
UPIACK-
RINT-
RRDS
RDAD
RDSTB-
QRST
QCLKI-
MRST
SRSTB-
WAIT-
RDY-
BSY-
PRBLM-
74LS241
74LS240
74LS20
74LS04
74LS109
74LS173
74574
74LS00
74LS08
74LS161A
7438
basic/four corporation
903031
SH 13 OF 15


WRITE STRØBE SYNCHRØNIZER
(2) QCLK1-
R10 (9E)
+5V
220
330
P2-48
WDS-
(11) TEST 19
RWDS
+5V
74LS109
N/C
QWST-
7A
74LS73
QWST1
QWST2
5A
74LS04
GWST2-
4A
74LS00
SWSTB-
(12)
(2) IØRD7-
(11) TEST-1
8B
74LS240
(2) MRST-
SWSTB-
(5) IORD7 19
(3) RDCT8- 15
UPD7 (4)
WRITE BIT CØUNTER
WCT8- 13
UPD6 (4)
3J
74LS241
WRITE DATA ENABLE LATCH
(11) TWDE
TWDE-
74LS04
4A
74LS00
SWSTB
CLK1
(2)
(3) MRINIT-
4B
PE
ENP
ENT
CLR
D
C
B
A
RL
QD
QC
QB
QA
74LS161A
3A
74LS08
WRWTØK
2B
7438
WAIT-
(2,10,13)
WCT8
(12)
(2) IØWR4-
GE
74LS04
IØWR4
WTNLD-
(12)
(2,13) INT-
+5V
GTWDE
(11)
1B
74LS09
N/C
MRST-
MTU WRITE TIMING
basic/four corporation
SIZE C
DWG NO 903031
REV D
SCALE NONE
SH 14 OF 15

P1

	A		B	
(1)	GND	1	+5V	(1)
(1)	GND	2	+5V	(1)
		3		
		4		
		5		
(10)	CPHI	6		
		7	MAI2-	(8)
		8		
(8)	MA07-	9	MAI4-	(8)
(4)	ØD05-	10	ØD01-	(4)
(8)	MA09-	11		
(8)	MA10-	12		
		13	MA11-	(8)
		14	MA08-	(8)
(8)	MA06	15		
		16		
		17		
		18	MA13-	(8)
		19		
		20	RTXX-	(10)
		21		
		22	CHP2-	(5)
		23	MREAD	(10)
(8)	HSDMA	24		
		25		
(4)	ØD02-	26	ØD06-	(4)
		27	MD07	(9)
		28	MD03	(9)
		29		
		30	MD05	(9)
(5)	I02X-	31	I01X-	(5)
(4)	ID04-	32	ID00-	(4)
		33	MAI6	(8)
		34	MD00	(9)
(9)	MD01	35		
(9)	MD04	36		
		37	ØD04-	(4)
(7)	EINT-	38		
		39	ØD00-	(4)
		40	MD06	(9)
		41	MAI7	(8)
		42		
		43	MD02	(9)
(10)	DMAR-	44	RESET-	(5)
		45		
		46		
		47	MAI5-	(8)
		48	DMACK-	(10)
		49		
(8)	MA03-	50		

P1

	A		B	
		51	MA00-	(8)
(7)	SEL0-	52	SELI-	(7)
(8)	MA04-	53	MA01-	(8)
(8)	MA05-	54	PRIN-	(7)
(7)	PROT-	55	MA02-	(8)
		56		
(10)	DMACK-	57	DMAI3	(8)
(4)	OD07-	58	OD03-	(4)
		59	ID05-	(6)
(4)	ID01-	60	ID07-	(6)
(6)	ID06-	61	I03X-	(5)
(4)	ID03-	62	ID02-	(6)
		63		
(1)	GND	64	+5V	(1)
(1)	GND	65	+5V	(1)

P2

1	GND	(10)
2	SLD-	(12)
3	GND	(11)
4	RDY-	(12)
5	GND	(11)
6	WND-	(12)
7	GND	(11)
8	FLG-	(12)
9	GND	(11)
10	LPS-	(12)
11	GND	(11)
12	FUP-	(12)
13	GND	(11)
14	BSY-	(12)
15	GND	(11)
16	EWS-	(12)
17	GND	(11)
18	RWD-	(11)
19	GND	(11)
20	REV-	(11)
21	GND	(11)
22	FWD-	(11)
23	GND	(11)
24	HSP-	(11)
25	GND	(11)
26	WEN-	(11)
27	GND	(11)
28	SLI-	(11)
29	GND	(11)
30	SL2-	(11)
31	GND	(11)
32	SL4-	(11)
33	GND	(11)
34	SLG-	(11)
35	GND	(11)
36	RNE-	(12)
37	GND	(11)
38	RDS-	(13)
39	GND	(11)
40	DAD-	(13)
41	GND	(11)
42	WDE-	(11)
43	GND	(11)
44	WNE-	(12)
45	GND	(11)
46	TR2-	(11)
47	GND	(11)
48	WDS-	(14)
49	GND	(11)
50	TRI-	(11)

basic/four corporation

SIZE	DWG NO	REV
C	903031	D

SCALE NONE SH 15 OF 15

Basic Four
Information Systems®

Service Manual Change Request

Prepared By: _____
Name Title

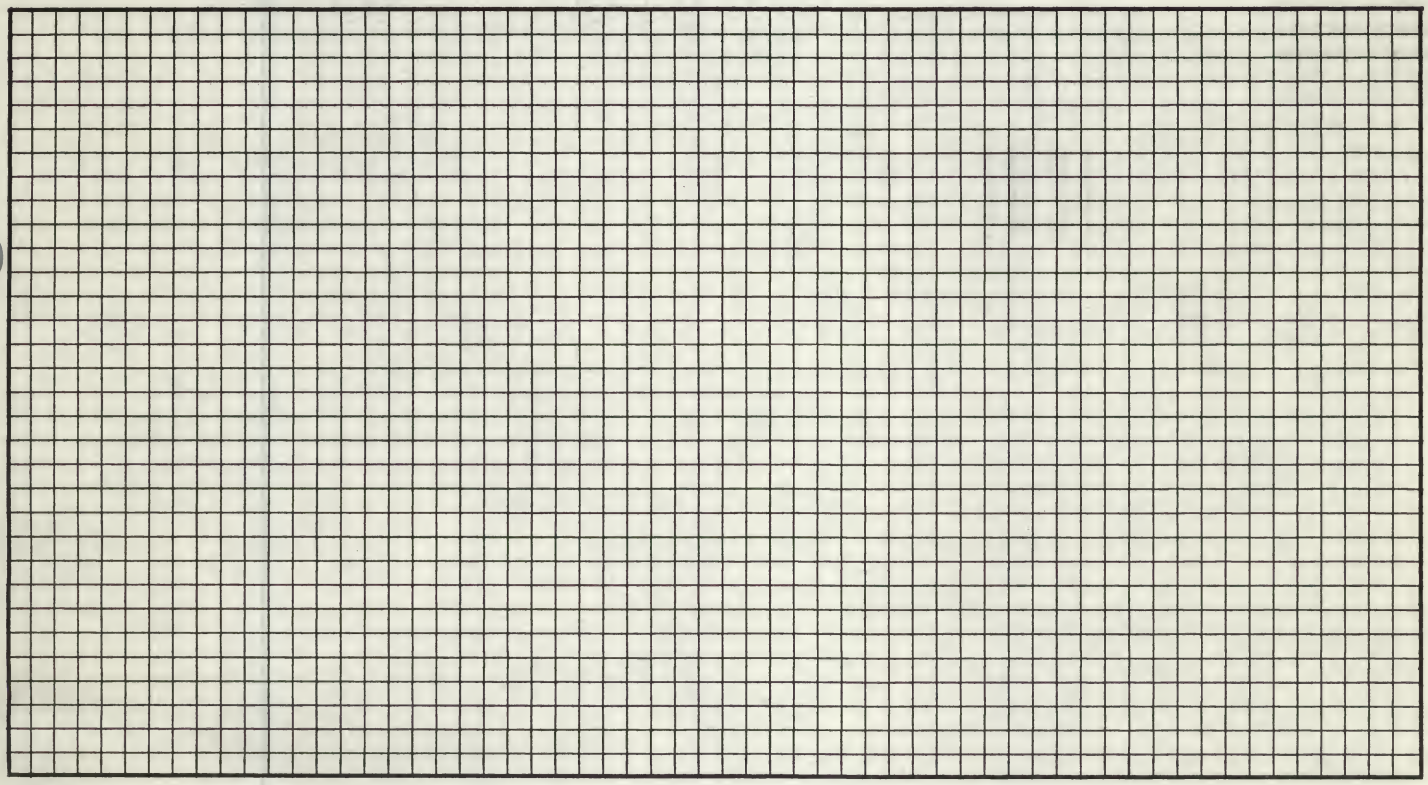
_____
Address

_____
Date

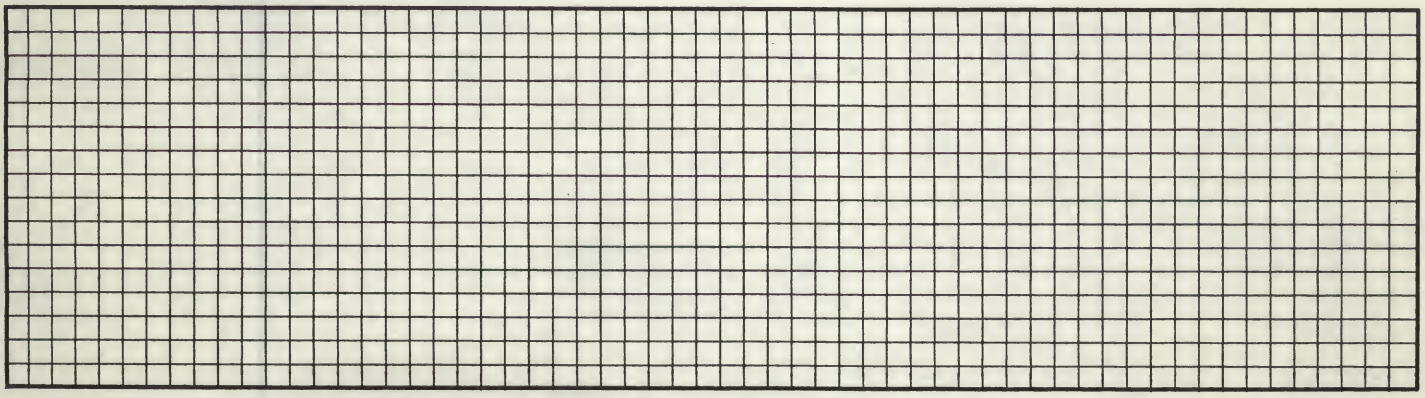
Manual No. _____ Equipment Covered _____

Pages affected _____

Description of requested changes



Reason for requested change



Fold and staple

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 4388 SANTA ANA, CA

POSTAGE WILL BE PAID BY ADDRESSEE

Basic Four Information Systems Division
Management Assistance Inc.
14101 Myford Road
Tustin, California 92680

Attention: Manager, Technical Publications Department